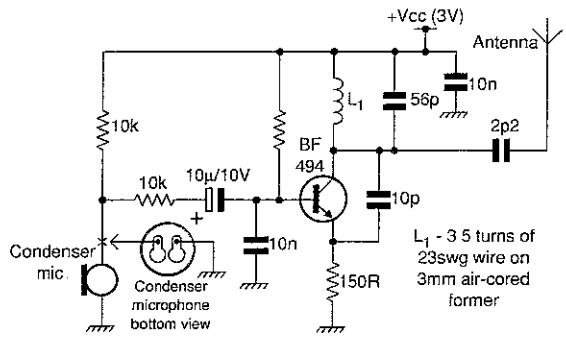
One transistor fm microphone



Running from two penlight cells, this sensitive fm microphone has a transmission range of around 6m. Lengthening the antenna could increase this to 30m.

Due to L_1, the *BF494* transistor oscillates in addition to amplifying the signal from the piezo microphone. Once the circuit is operational, tune an fm radio around 100MHz until the noise quiets.

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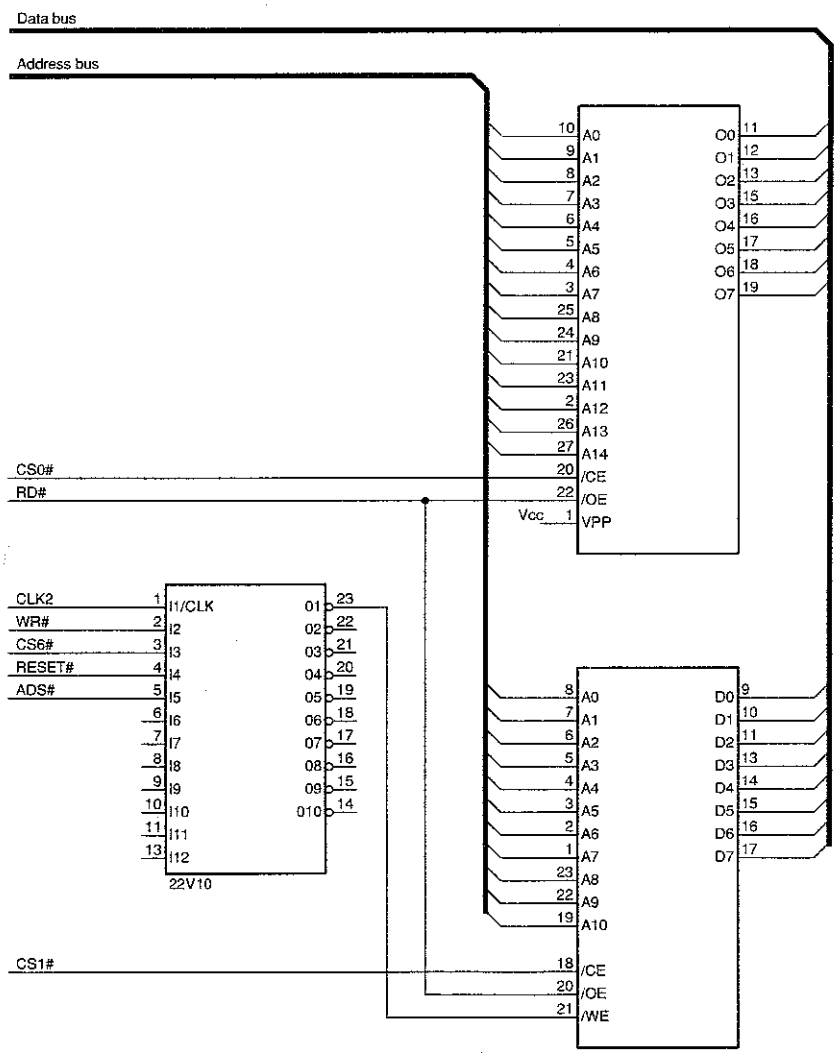
In this fm microphone, one transistor doubles as an audio amplifier and transmitter oscillator.

Write protect for 386EX architectures



In this example, part of a circuit for write protecting memory in 386 systems, /CS0 enables the eprom, /CS1 enables the ram and /CS6 defines the write-protect address range.

In system designs using an embedded processor, it is often useful to include a 'write-protect' circuit for part of the read/write memory. This may be to safeguard configuration parameters, or simply for debug purposes.

However, it is difficult to predict exactly which areas of ram will need to be protected, and ideally the protected area should be configurable by software, so the design can be problematic.

This circuit is a mechanism for a versatile write-protect system which may be implemented in almost any design using the Intel *386EX* processor. It can often be included without adding to the component count.

Intel's *386EX* processor includes a powerful chip select unit (csu) which may be programmed to provide fully decoded address blocks for memory or i/o devices; it has seven independent outputs, so most designs will not need to use them all.

In addition, the csu allows more than one output to be active during any bus cycle, although this would normally be avoided to prevent address-decode clashes. It is therefore a simple matter to gate the processor's /WR line with a spare csu output before feeding it to the memory subsystem. This csu output is then programmed to be active only when a block of ram which is to be write protected is simultaneously addressed (in the normal way) by a different csu output.

The write protected area may then be set to cover any memory address range, subject only to the limitations of the csu itself, and it may be enabled, disabled and reprogrammed entirely by software.

The current version of the *386EX* (the 'B' step) has a number of deficiencies, one of which is an insufficient address hold time after /WR is removed. A common method of overcoming this problem is to use a PAL to foreshorten the /WR pulse, often in conjunction with a simple state machine to track the processor 'T' states. Feeding a spare csu output into this PAL is then a convenient way of implementing the write protect mechanism described above.

The diagram shows a simplified extract from a circuit which embodies this function. No doubt the scheme could be adapted to suit other processors which include a similar chip-select unit.

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