A NEW GENERATION OF ANALOGUE SWITCHES

by Jack Armijos and Tania Chur*

Most applications for analogue switches fall into two categories: signal routeing and signal conditioning. Different processing technologies produce switches with different characteristics. One advantage of the new CMOS analogue switches from Siliconix is that they allow you to control signals that fall anywhere between the two power supply rails. Furthermore, these

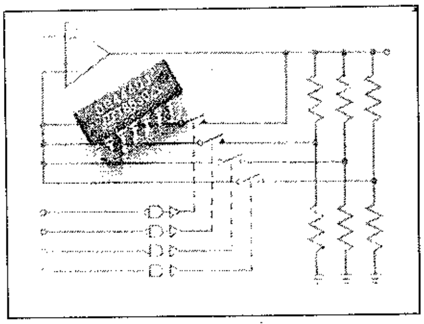

Fig. 1. The DG400 series of analogue switches

high-performance silicon-gate ICs, the DG400 family are pin-for-pin replacements for the popular DG200 series. They offer significantly lower on-resistance ($r_{DS(on)}$=85 Ω), lower power dissipation (35 μW), faster switching speed (t_{on}= 250 ns) and lower leakage current ($I_{S(off)}$ <500 pA) than the older industry-standard parts. The new devices are shown here in typical circuits, illustrating the benefits they offer.

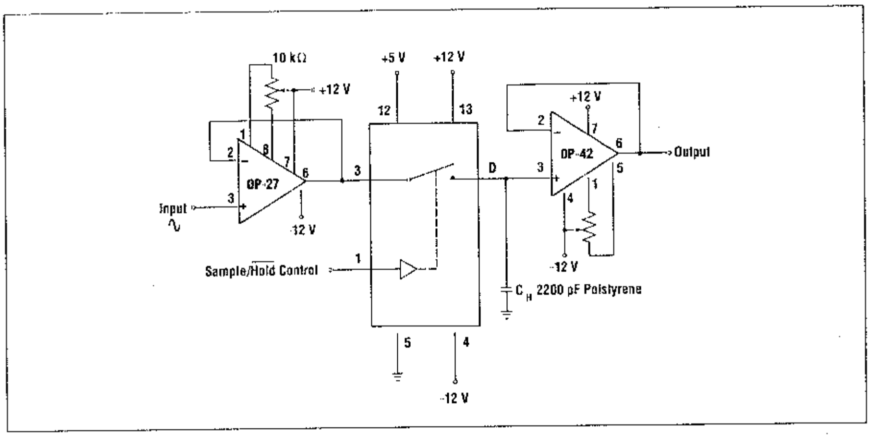

Fig. 2. Open-loop sample-and-hold circuit uses a fast analogue switch

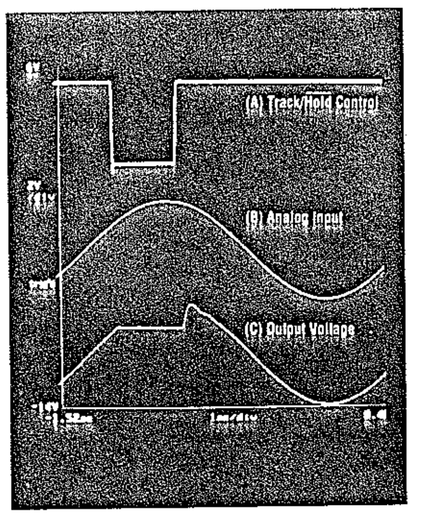

Fig. 3. A logic LOW opens the DG412, placing the circuit in the hold mode

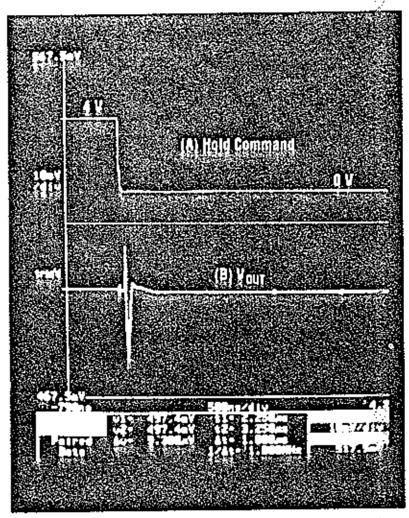

Fig. 4. V_{out} showing the effects of charge injection

Sample-and-hold functions

In most data acquisition systems, many channels are sampled sequentially and then digitized by an analogue-to-digital converter. In choosing or designing a sample-and-hold system, speed and accuracy are the two most important considerations.

Open-loop, cascaded-follower sample-and-hold circuit

The basic sample-and-hold circuit of Fig. 2 has unity-gain buffers to charge the capacitor without loading the signal source and to drive the next stage without changing the voltage stored. The basic operation of this circuit is illustrated in the photograph of Fig. 3. This configuration provides fast acquisition times and is good for high-speed acquisition systems.

The input buffer is chosen for low offset voltage, good slew rates, and the ability to drive the capacitive load. A polystyrene capacitor is used because of its very low dielectric absorption and low leakage. The output buffer needs to have a short settling time and very low input bias to prevent the discharge of the hold capacitor during the hold mode.

The most important switch parameters are: speed, to minimize the acquisition time (fast throughput); low charge injection, to reduce the hold step error; and low leakage to maintain a low droop rate. The DG412 offers improvements for all three areas of performance.

The circuit shown in Fig. 2 achieved an acquisition time of under 900 ns and a droop rate of 10 μV/μs. Pedestal error was a function of analogue signal voltage. The worst-case error was 23 mV when V_{in} = 5 V.

The photograph in Fig. 4 shows V_{out} immediately after the hold command. In this case, V_{in} = 0.5 V. Note the upset caused by the charge injection of the switch when it opens, the offset error that

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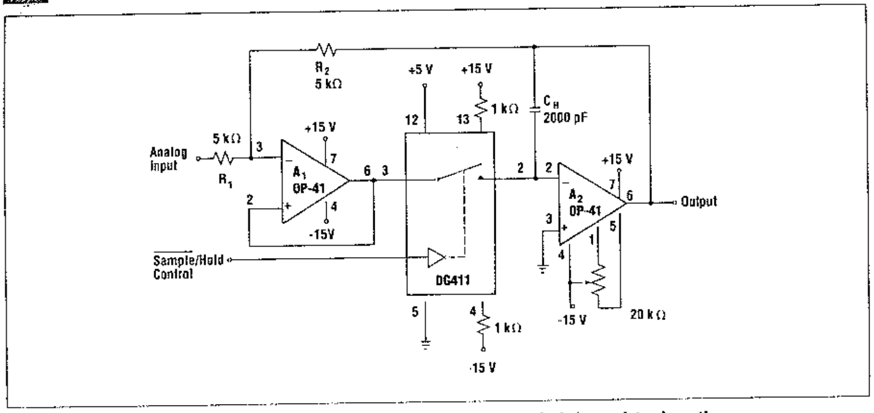

Fig. 5 Integrator output sample-and-hold function operates switch into virtual earth

remains after the upset and the droop rate that begins after settling is completed.

Closed-loop integrator output sample-and-hold circuit

A popular sample-and-hold configuration is shown in Fig. 5. This circuit is simple and accurate. It has a gain of –1 since $R_1 = R_2$. Opamp A1 acts as a current booster to speed up the charging rate of hold capacitor C_H. Since the unity-gain buffer has a very low output impedance, the time constant associated with C_H is determined primarily by the on-resistance of the switch and by the magnitude of the hold capacitor. Thus the circuit benefits greatly from the low on-resistance of the DG411.

The settling time of the output voltage is determined by the slew rate and settling time of the integrator stage. In the sample mode of operation, the DG411 closes and hold capacitor C_H charges to the negative of the input voltage. In the hold mode, the analogue switch opens after the capacitor has acquired this voltage to the desired accuracy. Another advantage of the DG411 is that the switch always operates at a virtual earth potential regardless of the input voltage. Since at this level the charge injection on the switch drain is at its minimum value, the hold step error is minimized. The errors of A1 are minimized in the sample state, although they do appear in the hold mode.

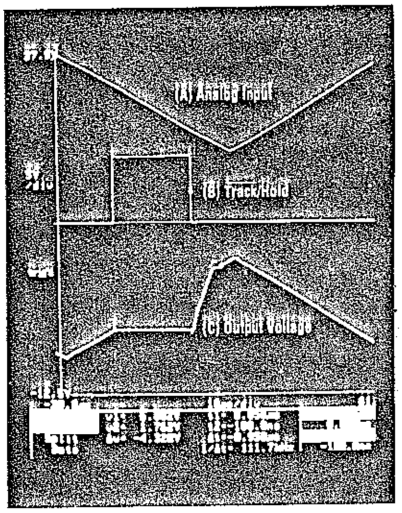

Fig 6. Acquisition time is limited by the slew rate of the output amplifier

The photograph in Fig. 6 shows the typical waveforms associated with this circuit. With the components shown, this circuit achieved an acquisition time of about 20 µs, a maximum hold step error of 3.8 mV and a droop rate of 7.5 µV/µs.

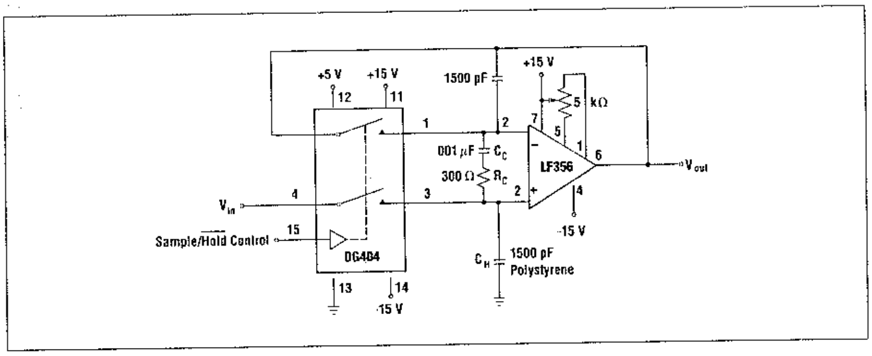

Fig 7. Fast and precise sample-and-hold circuit

Fast and precise sample-and-hold circuit

The circuit shown in Fig. 7 uses a DG404 analogue switch in conjunction with a JFET input operational amplifier. The DG404 is a fast switch (T_{on}<150 ns). In this circuit, both switches have a similar potential when open, so their charge injkection effect is minimized by their differential effect on the opamp. Acquisition time of this circuit was less than 600 ns, worst-case pedestal error was –5 mV and droop rate was 35 µV/µs.

The compensation network formed by C_C and R_C helps to reduce the hold-time glitch and optimizes acquisition time. The photograph in Fig. 8 shows this circuit's output without a compensation network. Notice the large glitch going into the hold mode, as well as the rippled waveform right after the output slews to its new value at settling time. The photograph in Fig. 9 shows the improved response after the compensating network has been installed.

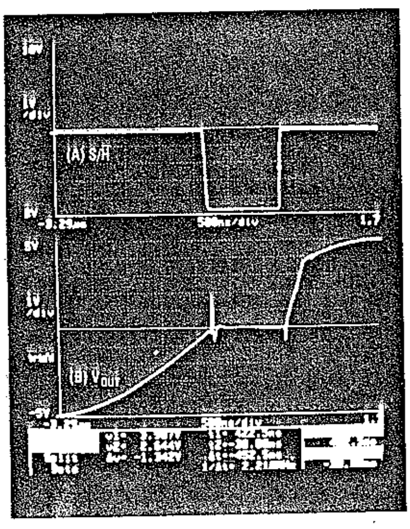

Fig. 8. V_{out} without compensation shows large glitches and a waveform ripple during acquisition time.

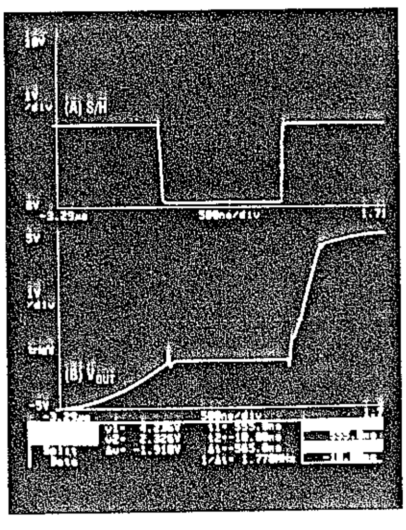

Fig. 9 Improved V_{out} after compensation.

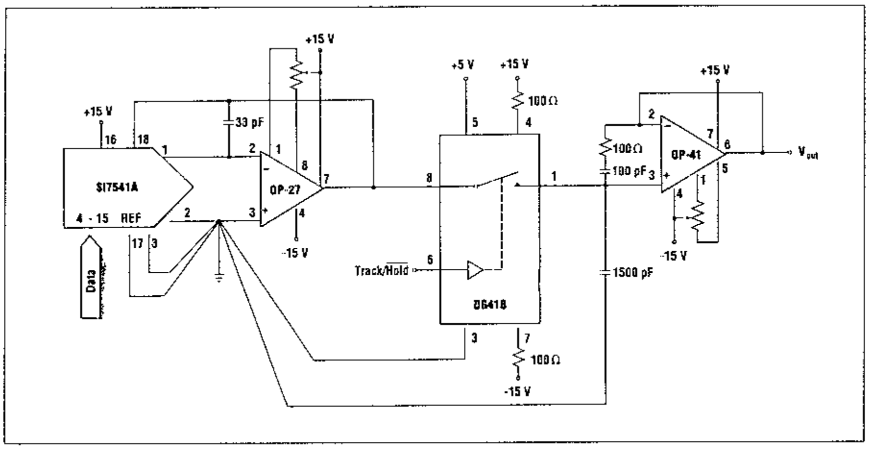

Fig. 10. Digital-to-analogue converter deglitcher.

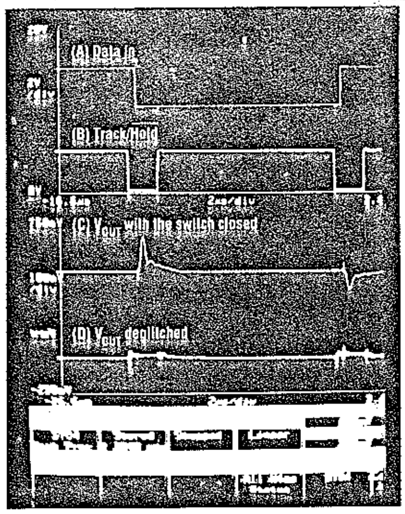

Fig. 11. Digital-to-analogue converter deglitcher waveforms

Digital-to-analogue converter deglitcher

Major code transitions in digital-to-analogue converters (DACs) can cause unwanted voltage spikes, commonly called glitches. In many DAC applications, these glitches can not be tolerated. Additionally, DACs from different vendors have different size glitches. (Note the glitch impulse specification on DAC data sheets.) To ensure a smooth transition when the DAC goes from one voltage to the next and to guarantee uniform circuit response regardless of alternate-sourced DACs, the DAC output may be processed with a tack-and-hold as shown in Fig. 10. While the DAC input code is unchanged, the DG418 is closed and V_{out} tracks the output of the current-to-voltage converter. Just before a code change occurs, the analogue switch is opened so that V_{out} continues showing the previous voltage. After the code change and its associated glitch has settled, the DG418 closes again and the track mode is resumed.

The photograph in Fig. 11 shows V_{out} with the DG418 always closed (c) and with the deglitcher active (d). Notice the improvement in the transition glitches.

The DG418 offers high switching speeds, which are required for short conversion times, and low charge injection which minimizes pedestal errors.

Dual-input programmable gain amplifier

For digital systems where only a +5 V supply is available, a small amount of analogue processing can be implemented with a low-voltage converter IC and low-voltage analogue components. Figure 12 shows an amplifier suitable for data acquisition or voice recognition applications where either of two analogue signals is selected and amplified by a very precise, self-calibrating chopper-stabilized amplifier. Circuit gain can be selected as either ×2 or ×10. A single DG423 analogue switch was used to perform both the input-select and gain-select functions. Its low on-resistance, high speed, and on-chip latches ease circuit design and improve overall accuracy.

The photograph in Fig. 13 illustrates the operation of the circuit. For demonstration purposes, input- and gain-selects were tied together so that when the 0.5 V (p-p) triangular signal was being processed, the circuit gain was ×10 whereas when the 3 V (p-p) sine wave was selected, the amplifier's gain was reduced to ×2. This type of gain ranging is useful to precondition analogue signals of different amplitudes prior to an analogue-to-digital conversion.

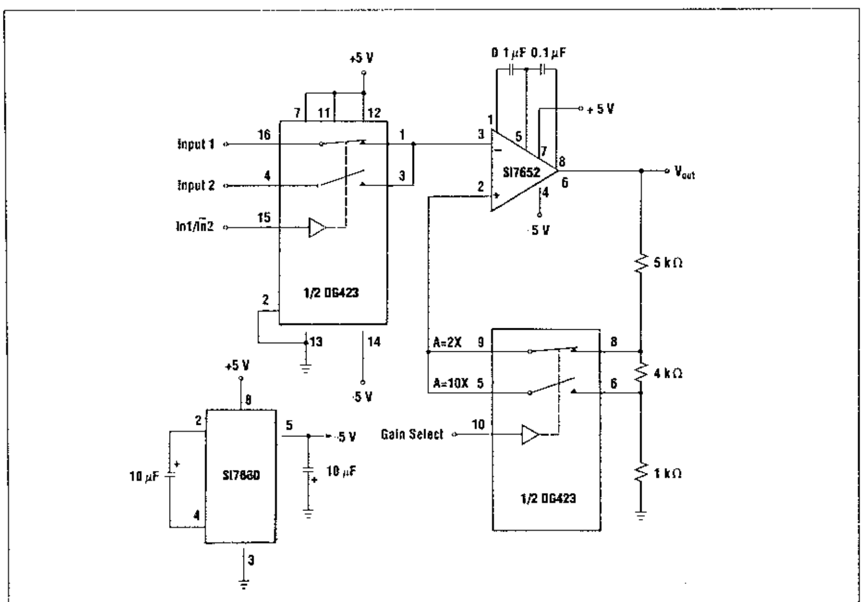

Fig. 12. Low-voltage programmable gain amplifier.

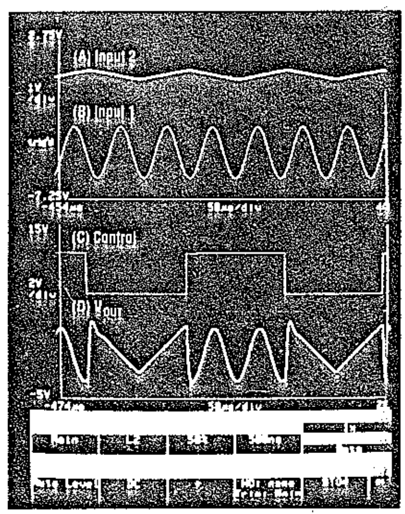

Fig. 13. Gain ranging produces similar amplitudes even if the input levels are different.

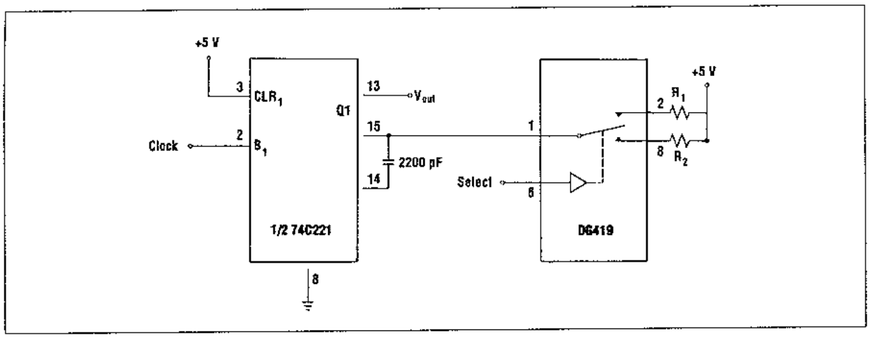

Fig. 14. Programmable one-shot multivibrator.

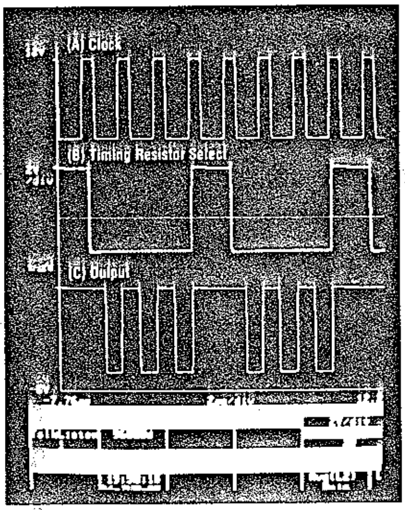

Fig. 15. A logic LOW produces short pulses and a logic HIGH creates long ones

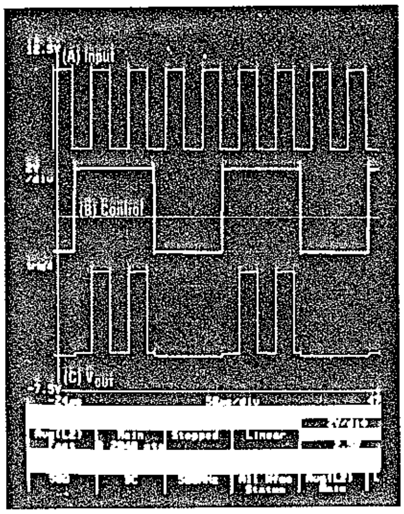

Fig. 16. This photograph illustrates the remote switch-over action

Programmable one-shot multivibrator

Another useful application for an analogue switch a programmable one-shot multivibrator is shown in Fig. 14. This circuit produces pulses whose duration is determined by digitally selecting one of the two timing resistors—see Fig. 15. Advantages of the use of the DG419 in this circuit are: small size (8-pin miniDIP or small-outline package) high speed low on-resistance and TTL compatibility even in single-supply operation.

Analogue switch powered by input signal

The analogue switch in Fig. 17 derives operating power from its input signal, provided that the amplitude of that signal exceeds 4 V and the frequency is greater than 1 kHz. This circuit is useful when signals are to be routed to either of two remote loads. Only three conductors are required: one for the signal to be switched, one for the control signal and a common return.

A positive input pulse – see Fig. 16 – turns on clamping diode D_1 and charges C_1. The charge stored on the capacitor is used to power the chip; operation is satisfactory because the switch requires a supply current of not greater than 1 µA. Loading of the signal source is imperceptible. The DG419's on-resistance has the respectable value of 100 Ω for an input signal of 5 V.

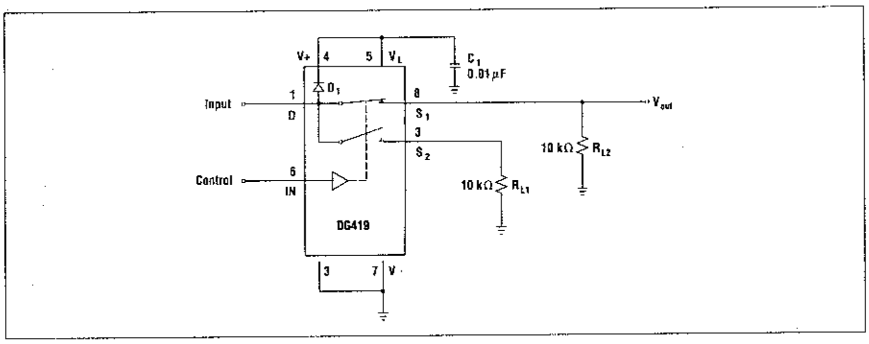

Fig. 17. Remote SPDT analogue switch for switched signal powers

Read/write disk-drive circuit

The circuit shown in Fig. 18 allows data to be written to or read from a disk. In the write mode, SW2 is closed. A ONE is created by momentarily closing SW1. This causes current to flow in the left-hand half of the head coil. A ZERO is produced when SW3 is closed. This causes current to flow in the right-hand half of the coil and reverses the direction of the magnetic flux.

In the read mode, switches SW4 and SW5 are closed. This connects the head coil to the read preamplifier so that the voltages picked up by the head as the disk glides by can be amplified.

Single-supply operation with +12 V, low-on resistance and high switching speed allow an improvement in data rates of roughly ×10 when DG411s are used in place of the more mature DG211s.

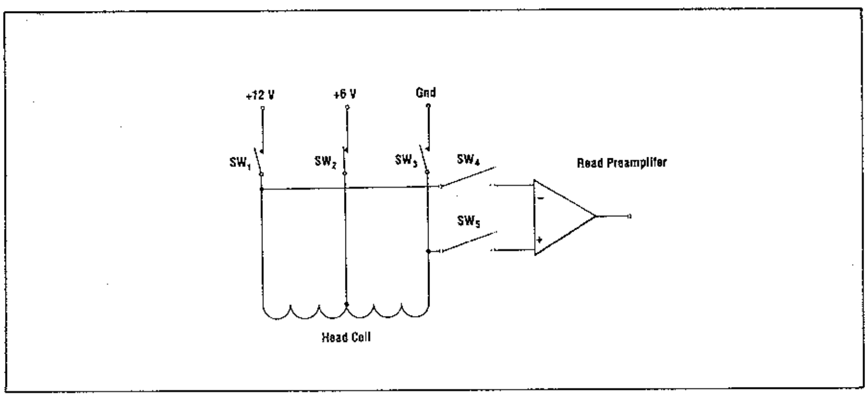

Fig. 18. DG411s in the head switching circuit of a disk drive

Micropower UPS transfer switch

The purpose of the uninterrupted power supply (UPS) circuit in Fig. 19 is to preserve volatile memory contents in the

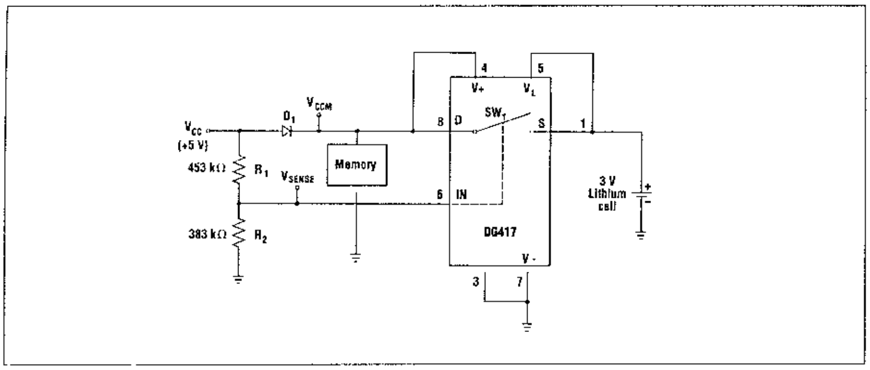

Fig 19. Micropower UPS circuit.

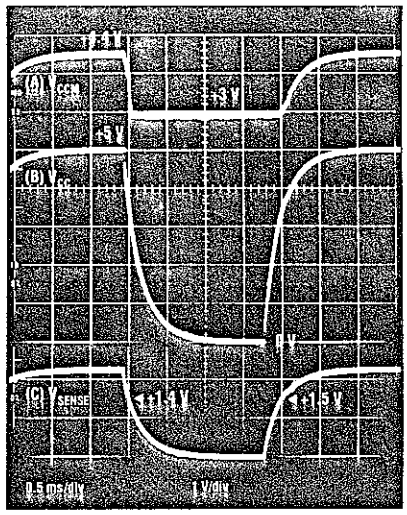

Fig. 20. Oscilloscope waveforms show a clean power switch-over

event of a power failure. In this application, every tenth of a volt counts. This circuit uses a micropower analogue switch that comes in an 8-pin miniDIP or small-outline package, a 3-V lithium cell to supply back-up power a diode and two resistors. Voltage losses under 0.1 V can be achie-ved

During normal operation currents of several hundreds milliamperes are supplied from V_{CC}. In this mode SW1 is open, so that the only drain from the lithium cell consists of leakage currents flowing into the V_L and S terminals. The leakage current is typically about 10 pA. Resistors R_1 and R_2 are continuously sampling V_{CC}

When V_{CC} drops to 3.3 V, the DG417 changes states closing SW1 and connecting the back-up cell. Diode D_1 prevents current from leaking back towards the rest of the circuit. Current consumption by the CMOS analogue switch is around 100 pA: this ensures that most of the available power is applied to the memory where it is really needed. In the stand-by mode, currents of some hundreds of milliamperes are sufficient to retain data.

When the +5 V supply comes back on, the potential divider senses the presence of at least 3.5 V and causes a new change of state in the analogue switch, restoring normal operation

On-resistance is about 74 Ω when V_{CC} is +5 V and 128 Ω when V_{CC} is +3 V. For example, an 800 µA load, equivalent to a static RAM of 256 kbit (MCM61L16), will produce a voltage drop of 0.1 V on the analogue switch, which is much better than the 0.6 V drop occurring if a simple 2-diode circuit were used

Higher currents and lower losses can be achieved by paralleling several sections in a multiple analogue switch such as the DG403

Line a in the photograph in Fig 20 illustrates how, in spite of V_{CC} dropping to 0 V (line b), uninterrupted power is applied to the load. Negligible voltage loss is caused by the switch. Line c shows that the DG417 changes state when its control input voltage decays to 1.4 V and changes again when it reaches 1.5 V on its way back to normal. The values of R_1 and R_2 may be adjusted for different trip points if desired

For the applications mentioned in this article, the DG4090 family of silicon-gate CMOS switches comes a step closer to the ideal switch. Any application that uses industry-standard analogue switches can now be improved by choosing these fast, lower-power, versatile analogue switches

ELECTRONICS SCENE

Course for the Radio Amateurs' Exam – May 1990

There will be a course for the May 1990 Radio Amateurs' Exam at Newark Technical College, Chauntry Park, Newark, Notts, starting this month on Monday evenings from 7 to 9 p.m. The course tutor is Alistair Morrison G4YZG

Further details may be obtained from Bert Drury G1UMK at the college, telephone (0636) 705921.

Radio Amateurs' Course

North Trafford College, Manchester is again offering a Radio Amateurs' Course starting this month. The course will comprise:

Theory	Thursday evening or Wednesday morning
Morse Code	Tuesday evening or Wednesday afternoon
Amateur TV	Wednesday morning
Advanced Morse Code	Monday evening

Lecturer: J.T. Beaumont G3NGD

Enrolment dates are 6, 7 and 8 September. Further details from North Trafford College of Further Education • Talbot Road • Stretford • Manchester M32 0XH • Telephone 061 872 3731

New Showroom for Nevada

Nevada the specialist suppliers of Communications, Music and Discotheque equipment have opened a new showroom in Portsmouth, adjacent to their present premises at 189 London Road, North End, Portsmouth PO22 9AE, telephone (0705) 662145.

In the new showroom, radio, scanner and short-wave enthusiasts will be able to browse in comfort with full 'hands on' facilities over Nevada's expanded range of products

New Maplin Store

Maplin Electronics, one of the fastest growing electronic retail groups in Europe, has recently opened another store in London.

The new store, managed by Lawrence Saunders, is located at 146-148 Burnt Oak Broadway, Edgware, Middlesex.

Further details from Maplin Head Office, telephone (0702) 552911