PLL SINE WAVE GENERATOR

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Precise frequencies that can be set very accurately are much more easily generated with the aid of digital technology than with analogue techniques. A snag with digital signals is, however, that their shape is rectangular rather than sinusoidal as required for many tests and measurements. The generator described in this article uses digital techniques, yet provides true sinusoidal signals

It is fairly simple to generate frequencies with the aid of, for example, an MS-DOS computer working with GW-BASIC. Without spending any extra money, every PC owner thus has a variable tone generator available. Unfortunately, the signal is rectangular and, therefore, not suitable for a number of tests and measurements.

If the generator is to be used without a computer system, another source of digital reference signal is required. For a number of applications, a simple variable square-wave generator will be perfectly acceptable. Where greater accuracy is required, a stable crystal oscillator with preset scaler must be used.

Control of the VCO

The generator is based on a combination of a phase-locked loop (PLL), here a Type 4046, and an integrated function generator, Type XR2206.

The principle of a PLL is shown in Fig. 1. The two most important parts of a PLL are a phase (Φ) comparator and a voltage-controlled oscillator (VCO).

The VCO will oscillate when a signal at a given frequency is fed to it. This frequency is determined by an external *RC* network. The output of the VCO (2) is fed to one of the inputs of the phase comparator; the other input of this stage is provided with the reference frequency (1).

The output of the phase comparator (3) is the difference between the two input signals. It is invariably a rectangular signal of which the mark-space ratio depends on the phase difference between the two input signals.

A low-pass filter at the output of the comparator integrates the pulses, which results in a signal whose absolute level is directly proportional to the phase difference of the input signals. The output becomes constant at the instant the loop is locked; this normally occurs at a phase difference of 90°.

Technical specification

Input impedance	>10 MΩ
Sensitivity	1–12 V_{p-p}
Frequency range	500 Hz – 100 kHz*
	10 Hz – 1 kHz**
Output impedance	600 Ω
Harmonic distortion	0.5% (typical)
* S1 open	** S1 closed

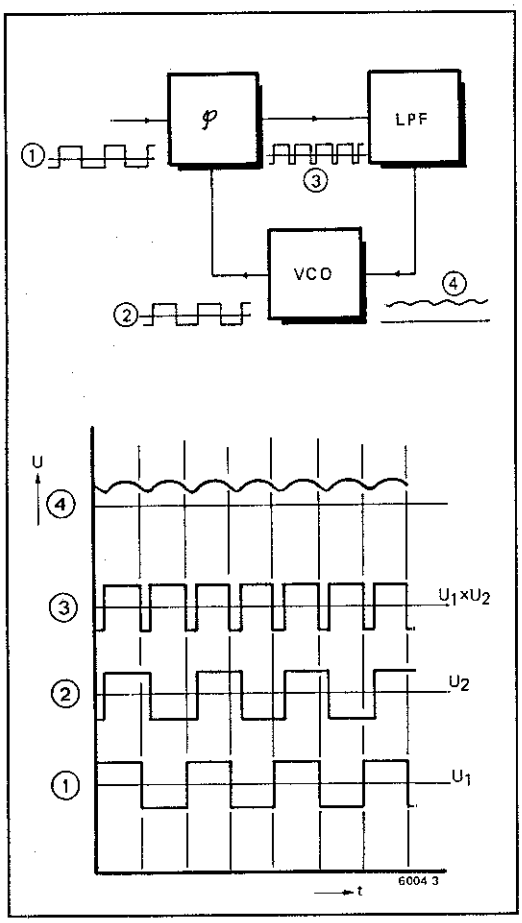

Fig. 1. Block diagram of a phase-locked loop (PLL).

As shown in Fig. 2, the 4046 used in the generator contains two different phase comparators. The first one of these is a single XOR gate, whose output is 1 if the levels of the two input signals are not equal. This comparator is not suitable for the present circuit because it requires symmetrical input signals and it will lock to harmonics of the input signals. Signals associated with this comparator are shown in Figure 3.

The second comparator is rather more complex and perfectly suitable for the present purposes. It is not sensitive to asymmetry of the input signals, since it operates on the edges of these signals. Moreover, it does not lock to harmonics of the input signals. This means that the sinusoidal signal is of exactly the same frequency as the reference signal. Associated signals are shown in Fig. 4.

An additional advantage of this stage is that it allows connexion to an LED that lights when the loop is locked to indicate that the output signal is as stable as the reference signal.

The output of the second comparator has not two but three states, depending on the input signals: 0, 1 or high impedance. The dependence of the output signal on the input signal is clear from Fig. 4. When the output of the comparator is high impedance it has no effect on the circuit following the comparator; it is, as it were, not present.

The period of time that the output is 1 or 0 depends directly on the phase difference between the input signal and the reference signal. If the input signal is first to have a leading edge, that is, is in advance of the VCO signal, the output becomes 1. If the VCO signal is first, the output becomes 0.

The low-pass filter following the comparator converts the output pulses into a direct voltage. This voltage increases when the comparator output goes high; it remains constant when the comparator

output is high impedance; and it decreases when the comparator output goes low. This means that the direct voltage is directly proportional to the phase difference between the input signal and the VCO signal.

Since the direct voltage is used to control the VCO, the circuit stabilizes at a given set of conditions. In the present comparator that happens when the phase difference between the input signal and the VCO signal is 0° and not 90° as is usual in PLLs. Because of this, the VCO frequency is exactly the same, and as stable, as the input signal.

From rectangular to sinusoidal waveform

Even a cursory glance at the circuit diagram in Fig. 8 shows that instead of the VCO in the 4046 a separate VCO, formed by IC5, is used. This circuit, strictly speaking a function generator, has the important advantage that it pro-

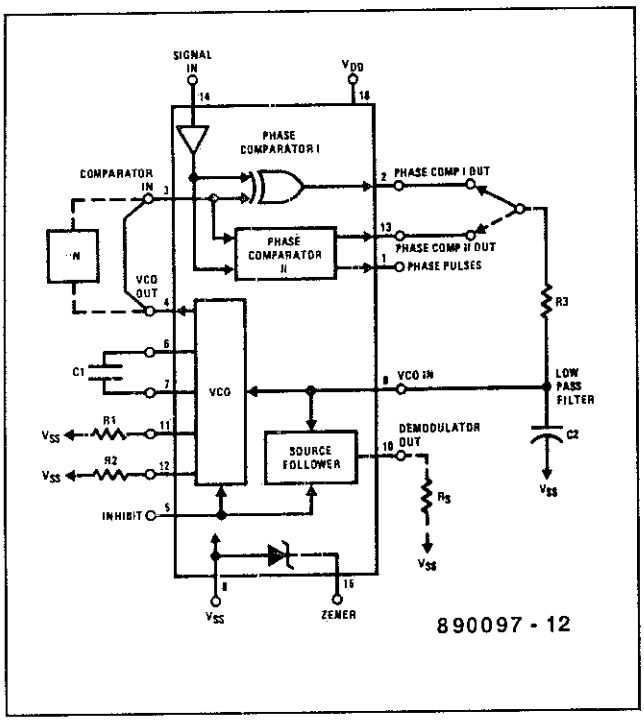

Fig. 2. Block diagram of the Type 4046 phase-locked loop (PLL).

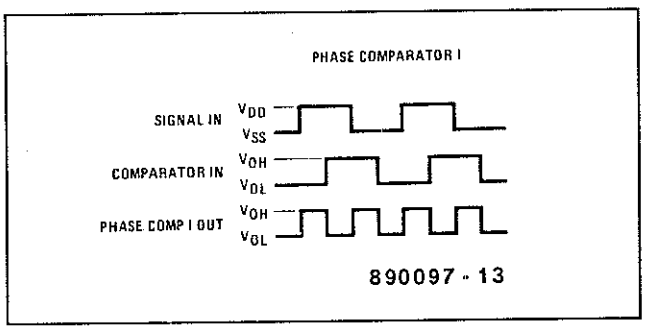

Fig. 3. Signals associated with phase comparator I.

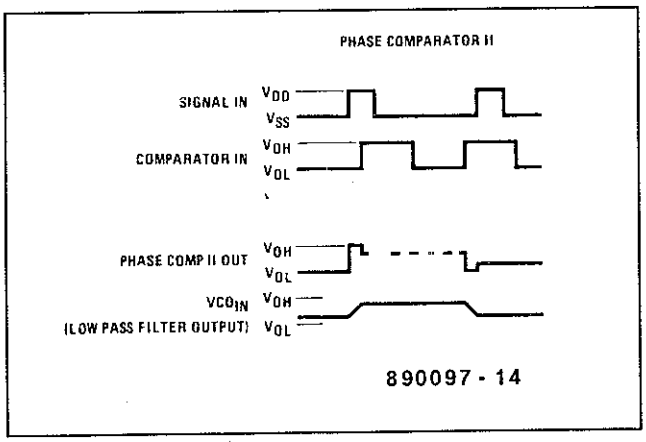

Fig. 4. Signals associated with phase comparator II.

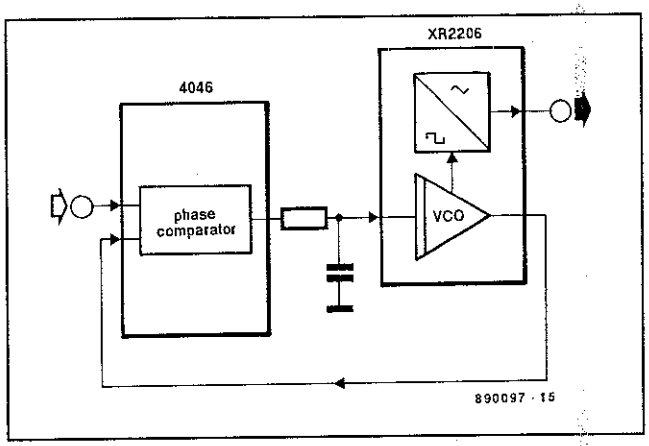

Fig. 5. Phase comparator II in the 4046 and the VCO in the XR2206 form a good-quality PLL.

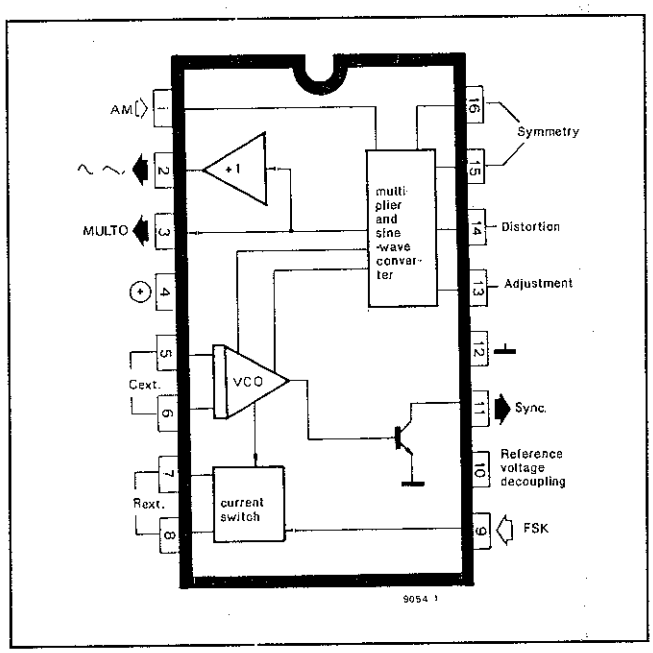

Fig. 6. Circuit diagram of the XR2206.

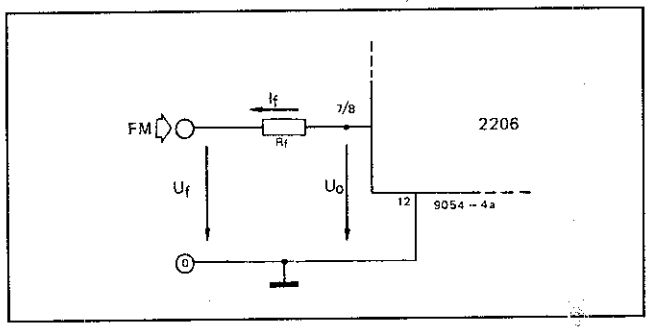

Fig. 7. The VCO input of the XR2206 is, strictly, a current-controlled output across which a fixed potential of 3 V exists. Applying a counter potential U_f via resistance R_f sets the input current.

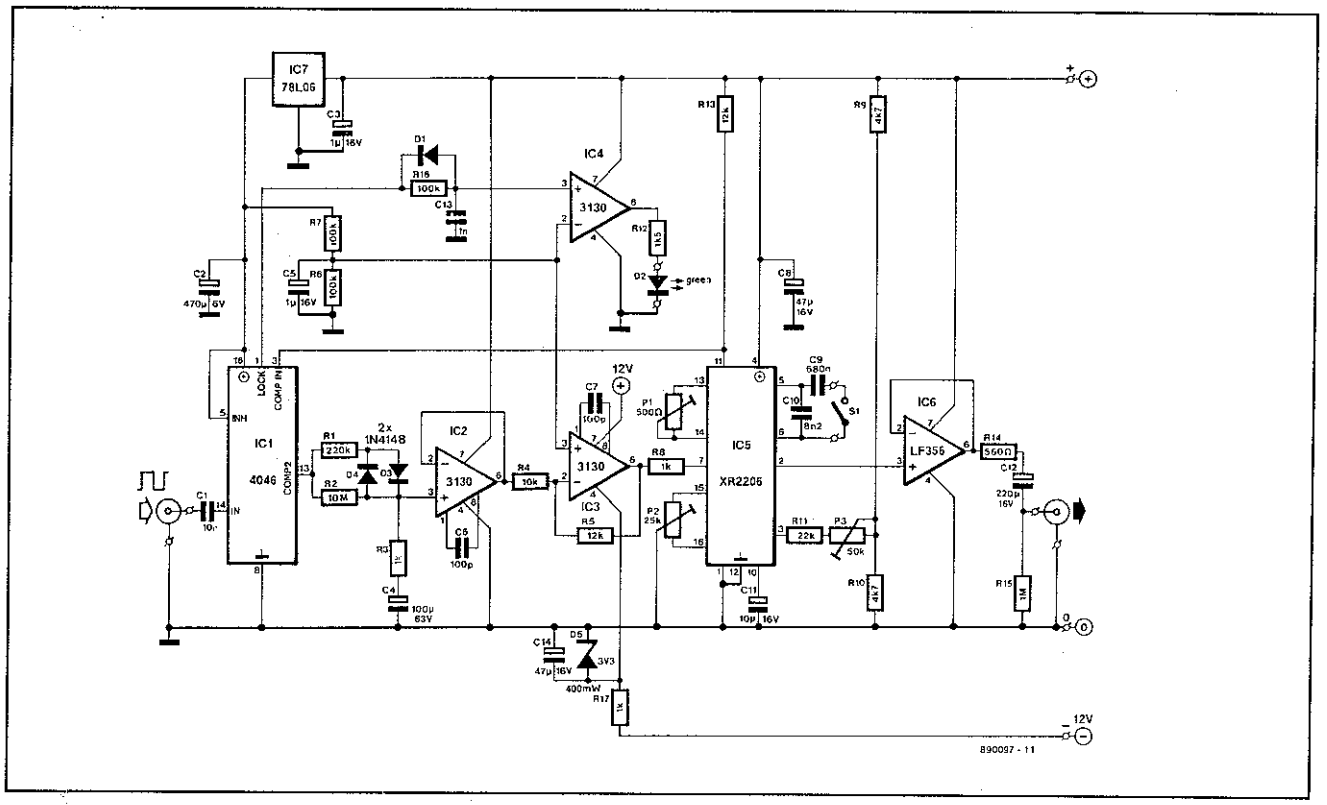

Fig. 8 Circuit diagram of the sine wave generator

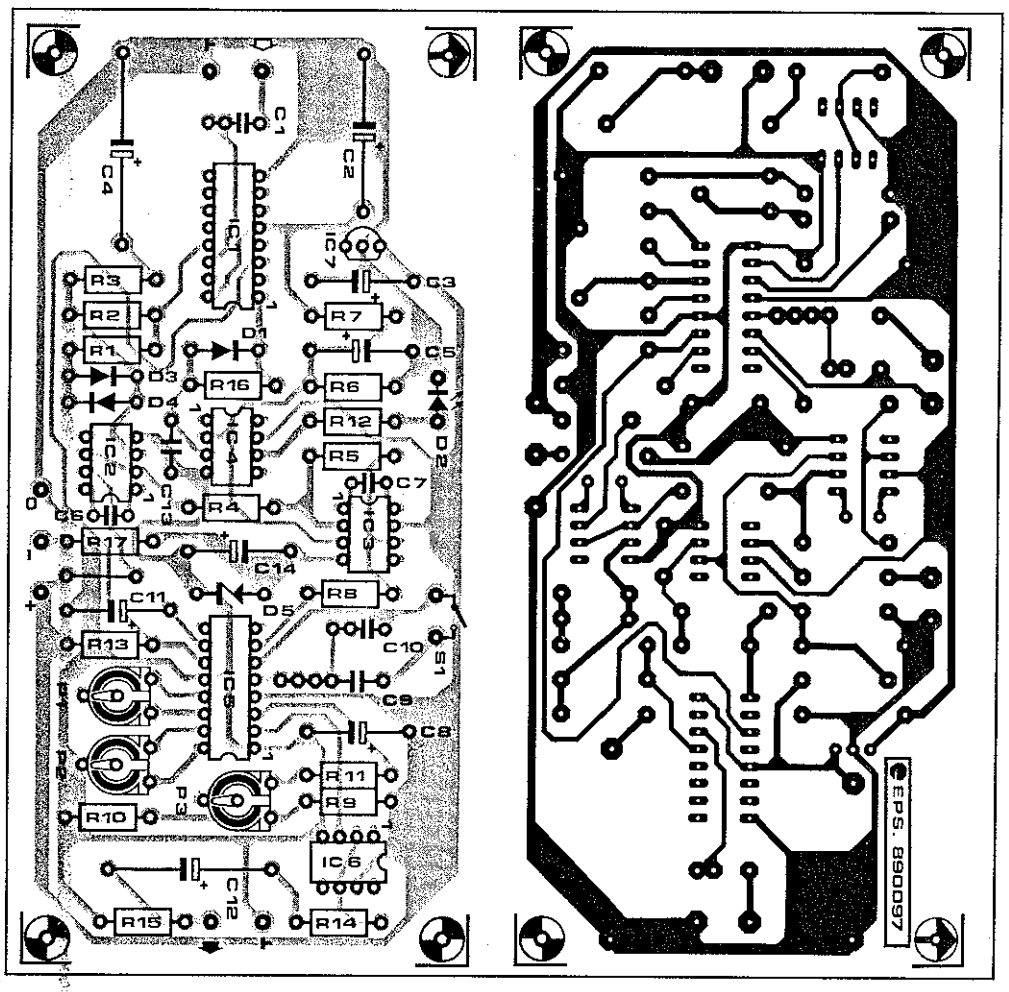

Fig 9 Printed circuit board for the sine wave generator

PARTS LIST

Resistors:
R1 = 220 k
R2 = 10 M
R3, R8, R17 = 1 k
R4 = 10 k
R5 R13 = 12 k
R6, R7, R16 = 100 k
R9, R10 = 4k7
R11 = 22 k
R12 = 1k5
R14 = 560 R
R15 = 1 M

Capacitors:
C1 = 10 n
C2 = 470 µ, 16 V
C3, C5 = 1 µ, 16 V
C4 = 100 µ, 16 V
C6 C7 = 100 p
C8 C14 = 47 µ, 16 V
C9 = 680 n
C10 = 8n2
C11 = 10 µ, 16 V
C12 = 200 µ 16 V
C13 = 1 n

Semiconductors:
IC1 = 4046
IC2 – IC4 = CA3130
IC5 = XR2206
IC6 = LF356
IC7 = 78L05
D1, D3, D4 = 1N4148
D2 = LED (green)

Miscellaneous:
S1 = SPST switch
PCB 890097-1

vides both a rectangular and a sinusoidal signal since it has a sine wave converter on board. Moreover, the IC remains perfectly reliable at low frequencies, so that it is truly linear over a wide range of frequencies.

The XR2206 is used in exactly the same way as that in the 4046 would have been. Its internal circuit is shown in Fig. 6.

Reverting to Fig. 8, opamp IC3 between the phase comparator and the VCO performs three distinct functions. In the first place, it inverts the control voltage for the VCO, because a decreasing voltage at pin 7 of IC5 would result in an increase in the output frequency. Secondly, its output signal has been arranged to allow it driving the VCO over its full range. Finally, the input of the VCO is controlled by a current rather than by a voltage. In other words, the control input of the VCO is in reality an output across which a fixed potential (U_o) exists and from which a current flows. The output voltage of IC3 determines the potential difference across R8 and thus the value of the current that will flow. The frequency f, is determined from:

$$f = (U_o - U_f) / (3 \times C \times R8) \quad [Hz]$$

in which U_o = 3 V; U_f = the output voltage of IC3; C = C10 or, if S1 is closed, C9+C10.

It may be calculated that, depending on the position of switch S1, a frequency range of 6 Hz to 125 kHz is available.

The remainder of the circuit is virtually nothing but the connexions between the various components.

The output of the phase comparator is connected to the VCO via low-pass filter R1-R2-R3-C4 and buffer IC2 in a manner that precludes any feedback to the comparator.

Diodes D3 and D4 shorten the time required by the circuit to lock by enabling the quicker charging and discharging of IC4. This is possible because at higher voltage levels R1 is connected in parallel with T2. This causes the impedance to decrease from 10 MΩ for small signals (PLL locked) to about 220 kΩ for large signals (PLL not yet locked).

Since the PLL may be used over a fairly wide frequency range, the low-pass section has a fairly large time constant to ensure good stability. Because of this, the PLL takes a relatively long time to lock. The 'acceleration' provided by the diodes is therefore welcome.

Diode D2, which is controlled by opamp IC4, lights to indicate that the PLL is locked. The opamp is connected to pin 1 of the PLL, which is specially provided for this purpose. A constant high level exists at this pin as long as the PLL is locked. As soon as the PLL tends to drift, small pulses appear at this pin and these are used by diode D1 to arrange for the fast discharge of C13. The voltage across C13 then drops to a level that causes the output of IC4 to become low. This in turn results in D3 being extinguished to indicate that the frequency is not stable.

Finally, a number of components are necessary for the proper functioning of IC5:

- resistor R8 and capacitors C9 and C10 determine the frequency range; S1 makes it possible to choose between the two ranges;
- resistors R9 and R10 set the d c operating level at the output (pin 2);
- preset P3 determines the amplitude of the output signal;
- preset P1 serves to shape the output waveform;
- resistor R13 is the collector resistor for the open-collector output of the VCO;
- circuit IC6 forms the output stage proper.

Construction and alignment

The circuit is intended to be built on the PC board shown in Fig. 9 and Fig. 10.

A number of soldering pins must be fitted on the board to facilitate connexions to other equipment.

The ICs may be soldered direct to the board.

With careful work, and particular attention to the polarity of the diodes and electrolytic capacitors, nothing should go amiss in populating the board.

Commence the alignment by setting all potentiometers to the centre of their travel.

Connect the output of the generator to an oscilloscope.

Apply a rectangular signal of 1 kHz, at a level of 5 V, to the input of the generator. As stated at the beginning of this article, this signal may emanate from a computer, simple square-wave generator or crystal oscillator.

Open S1 and connect an external ±12 V supply to the supply lines of the circuit.

If all is well, the oscilloscope should now show a reasonably well-shaped sine wave. If necessary, adjust P1 to make the signal as truly sinusoidal as can be judged. Once that is done, adjust P2 to make the signal look even better. Since the two potentiometers affect one another, the alignment must be carried out a few times. After correct alignment, the harmonic distortion is not greater than 0.5%.

The optimum position of P3 depends on the desired output level: be careful not to produce distortion of the output through overdriving.

If you prefer a continuously variable output level, that can be provided by a small modification. This consists of replacing R14 by two soldering pins. Connect a 1 kΩ potentiometer between the pin that is connected to the output of IC6 and earth. Connect the wiper of the potentiometer to the other pin. A continuously variable output signal is then provided via C12.

The suggested front panel shown in Fig. 11 should be given a calibrated scale to give a (relative) indication of the output signal. ■

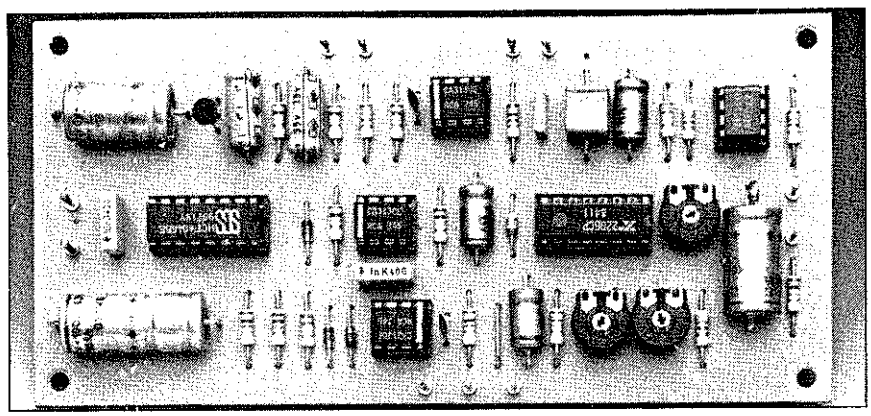

Fig. 10. Photograph of the completed printed-circuit board.

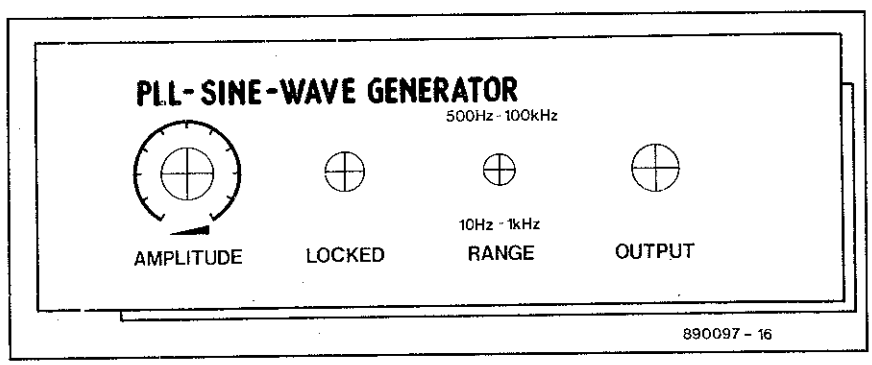

Fig. 11. Suggested front panel layout.