A HOME-BUILT FREQUENCY SYNTHESIZER FOR 45 TO 75MHz

John Crawley, GM3LBX*

THE CIRCUIT to be described is intended to be used as the heart of an up-converting receiver or transceiver covering the band from 100kHz to 30MHz. There have been considerable differences of opinion as to the advantages or disadvantages of using a synthesizer rather than a vfo in hf equipment, and I wish to demonstrate that a very reasonable synthesizer can be built by an amateur from parts which are easily obtainable. I also wish to remove some of the mystery from the whole subject!

The development of the system

The aim then was to provide the necessary injection frequencies for a double-superhet with a first i.f. at 45MHz, and a second i.f. at 455kHz. Clearly the first injection would need to vary from 45 to 75MHz, and it was decided to do this with a single tuning control and no band-switching. It would be more accurate to write "apparently no band-switching" because the thing does in fact work in such a way that the first loop in the system covers "bands" of 6·4kHz which are selected automatically by the state of the tuning control.

As with all synthesizers using digital circuits, the final frequency at the output changes in steps. The first decision which needed thought was what size the ultimate steps should be. Experience showed that steps of 10Hz produced a smoothness of tuning which seemed, even to my elderly ear, to be entirely acceptable. A little further thought resulted in the conclusion that to achieve such small steps across a 30MHz band was going to mean the use of at least two separate phase-locked loops. The ideal to aim at, was to make each loop share the work of dividing the final frequency down to the 10Hz, onto which the system would lock. We would then have something which would look like Fig 1.

Suppose that the vco in loop 1 is just a little over 45MHz and the vco in loop 2 is running at about 40MHz, then the resultant from the mixer would be around 5MHz; we would design the bandpass filter to pass 5 to 35MHz. The "divide-by-n" would be programmed to divide by 500 and the resulting 10kHz would lock with the 10kHz of the reference for this loop. The exact frequency of the output within the 10kHz which loop 1 has selected would be set by the frequency of the vco in loop 2. This would be arranged to vary in steps of 10Hz between, for example, 40MHz and 40·010MHz. If we were tuning upwards from 45MHz, the programming of

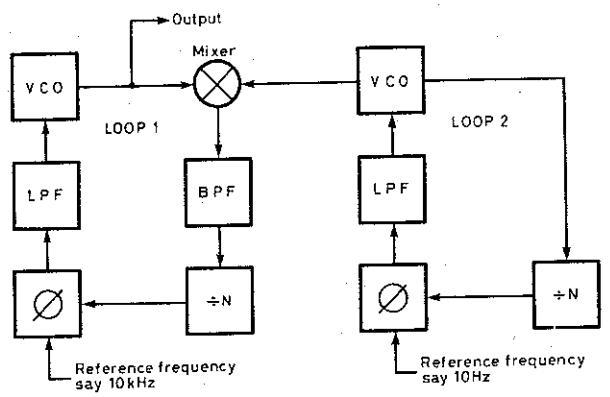

Fig 1. A basic arrangement

*Cove, Campbeltown Road, Tarbert, Argyll PA29 6SX

John L R Crawley was born in 1922 and educated in Liverpool. He served in the Merchant Navy, 1940–45 as a navigating officer with Thos and Jno Brocklebank, where friendly radio officers kindled in him a lasting interest in telecommunications. In 1949 he was ordained as a priest and is now retired. He was licensed in the 'fifties as G3LBX

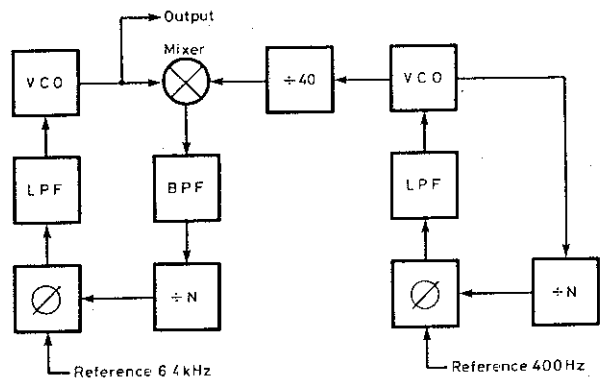

Fig 2. Achieving 10Hz steps with a 400Hz reference

the "divide-by-n" counter in loop 2 would be arranged to step from divide by 4 000,000 to divide by 4,001,000. But, of course, such high divisors would be complicated to achieve, and not possible with the parallel programming which had been decided on.

In fact the chosen device to do the phase-locking job was the MC145151. Since this is programmed in binary form and since certain divisors are available within the chip to provide a convenient reference frequency the step size (and therefore the reference frequency) for the first loop was to be 6·4kHz. This is easily arranged by providing a crystal at 3·2768MHz for the oscillator in the chip, and programming the internal reference divider to divide by 512 to give 6·4kHz; see Fig 2.

In the second loop a reference frequency of 10Hz was going to make difficulties in the lowpass filter; the solution was to think in terms of a step size of 400Hz and then to divide the vco frequency by 40. The interpolating frequency from loop 2 is to be mixed with the output from the vco in loop 1, and the difference frequency is to be divided down to 6·4kHz. Therefore, it is necessary for the loop 2 output to be within a few Megahertz of the lowest frequency required from the vco in loop 1. In fact the bandpass filter arrangements in loop 1 dictate that the best frequency for loop 2 would be about 40MHz. This would mean the vco in that loop running at 40 times 40MHz–1,600MHz! The answer is to use further mixing in loop 2. As there would, in any case be a need for a second injection frequency for the receiver of 44·545MHz, this could be doubled and mixed with the vco output in loop 2 (running between 95·3876 and 95·6432MHz). The resulting difference frequency of 6·2976 to 6·5532MHz could be filtered and used to feed the MC145151, while the straight 44·545MHz is mixed

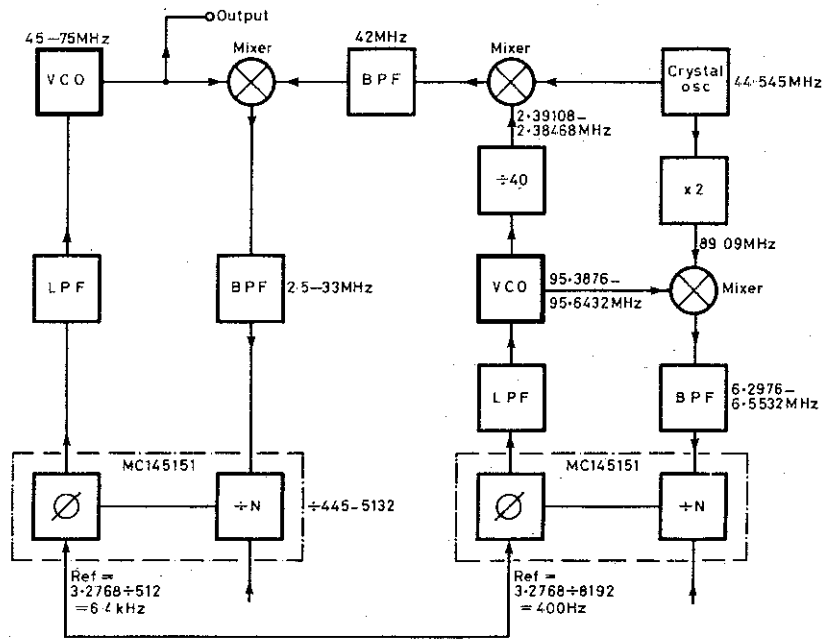

Fig 3 Block diagram of final arrangement

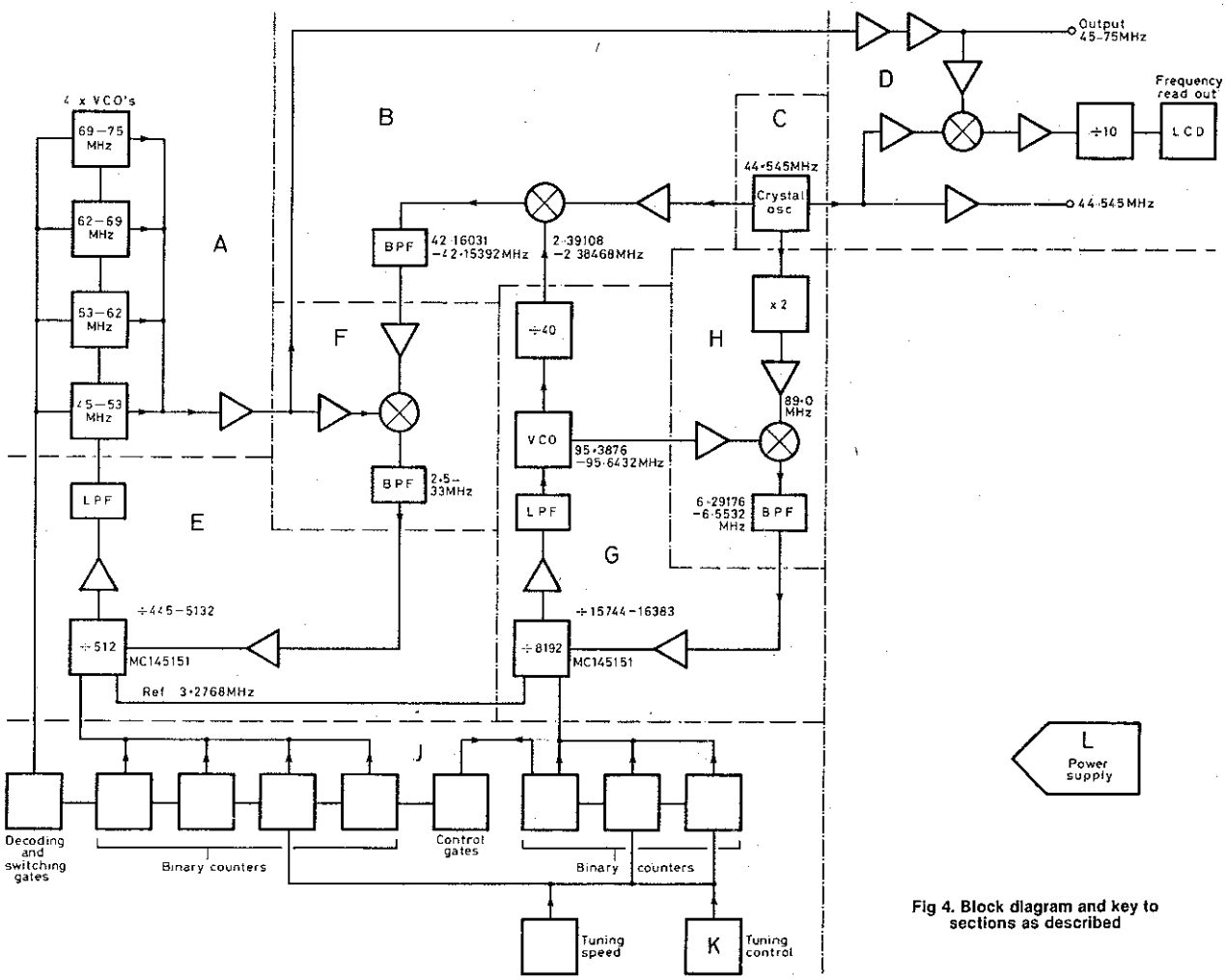

Fig 4. Block diagram and key to sections as described

with one fortieth of the vco frequency and the difference frequency (just over 42MHz) filtered and passed to loop 1. See Fig 3 for the final arrangement arrived at.

This arrangement has a lot of advantages. It keeps the vco in loop 2 well above the receiver passband and also above the highest output from the vco in loop 1. It also means that the range of frequency change in loop 2 is proportionally much smaller, so that the overshoot of the feedback necessary to produce the change from top to bottom of the range or vice-versa, is very much easier to limit.

The control circuit

The choice was made to use parallel input devices (MC145151) in order to be able to use a straight-forward tuning control which did not involve the complexity of microprocessors. The clearest approach seemed to be to use a string of binary counters, which has subsequently proved very reliable and trouble-free. The counters chosen are 74C193. They are run with a supply at +8V which they share with the rest of the control logic. IC908(a 74C02) provides for the counters, which programme loop 2 to count between 15744 and 16383, and also provides the carry or borrow pulses to increment or decrement the counter in loop 1.

The vcos in loop 1

In order to cover the whole range from 45MHz to 75MHz, there are four separate switched vcos in loop 1. By using very expensive varicaps you could get away with fewer, but there is little to be gained and you will need, in any case, to switch the front-end of the receiver. The status of the most significant bits in the 74C193 counter-chain is used to do the switching after decoding in IC909, 910, 911, an MC14012 and two MC14555s—these are Motorola versions of cmos 4012 and 4555.

Tuning control

It is convenient to be able to alter the tuning rate of a receiver, so the control pulses which originate in a shaft encoder are routed to one of three different points on the counter-chain. A push-button selects either *slow* (10Hz per pulse) *normal* (160Hz) or *fast* (41kHz). This allows the operator to move very quickly about the whole band, and then to select *normal* to look for signals and finally, *slow* to tune in the exact frequency required. The buttons are placed where the thumb of the "knob-twiddling" hand can find them most easily. A fourth button locks the frequency which has been selected.

Frequency display

An lcd is provided which displays receiver frequency. The resolution is to the nearest kilohertz. Obviously a larger display could be used. It would be nice to have another digit, but I was (and still am) counting the pennies.

BFO

In the prototype a third loop was used to generate the necessary 455kHz bfo injection. However, it was decided that the extra board space and component cost was not justified. There are, anyway, many good ways of getting 455kHz. I leave it to the reader to choose.

The circuit described by sections

Section A. The four vcos (Fig 6)

The four vcos are all alike apart from the inductances and C112.

(1) 45–53MHz approximately. L101 is eight turns 28g wire on Toko 10K former with adjustable core, but with no pot-core. C122 is omitted.

(2) 53–62MHz. L101 is Toko Style MC120 100079. C122 is 6·8pF.

(3) 62–69MHz. L101 is Toko MC120 100076. C102 is omitted.

(4) 69–75MHz. L101 is Toko MC120 100075. C122 is 4·7pF.

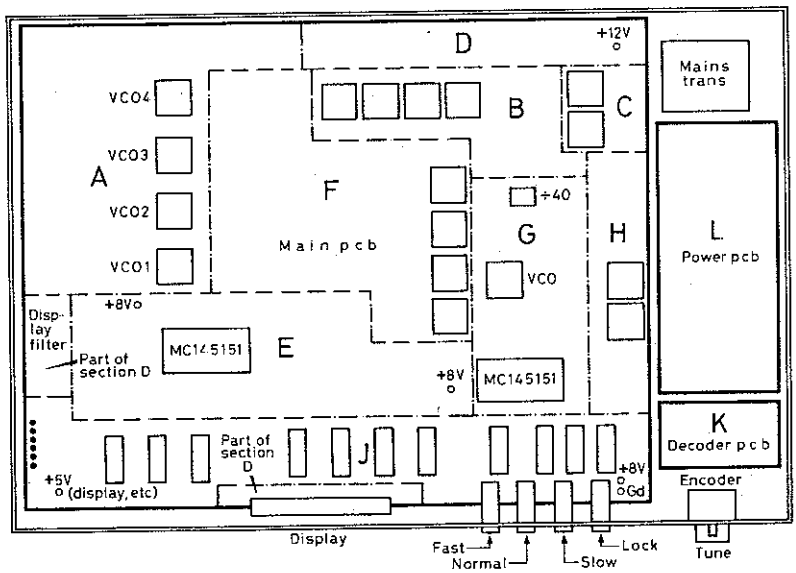

Fig 5. Plan of enclosure and pcb sections

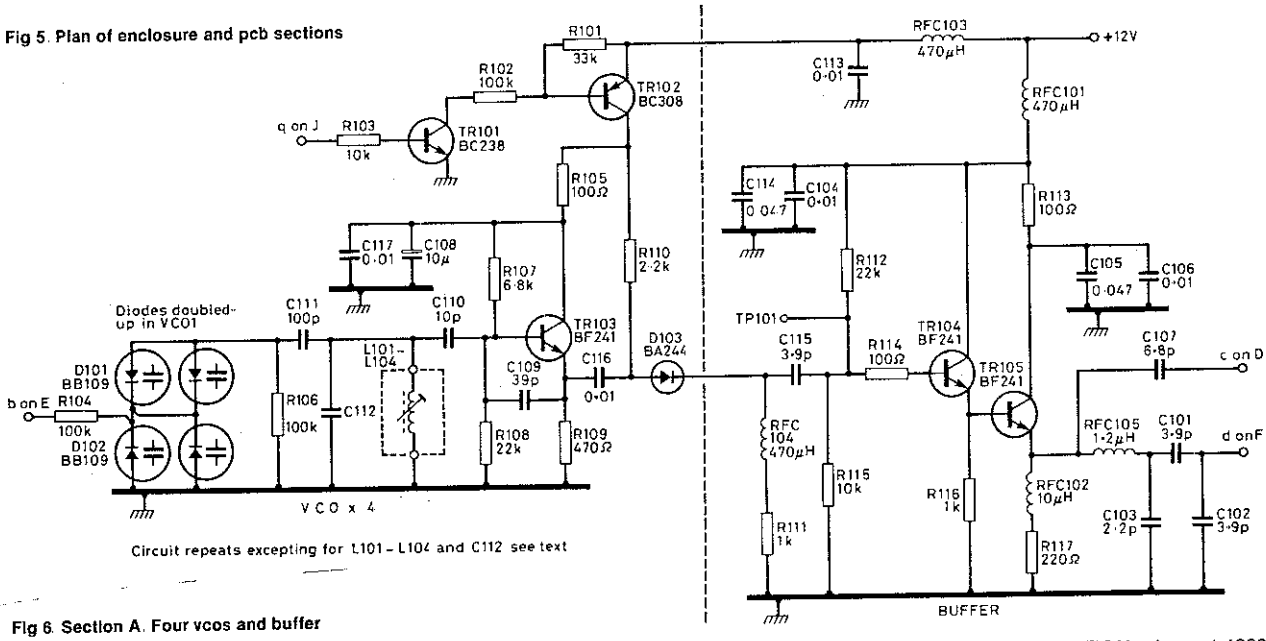

Fig 6. Section A. Four vcos and buffer

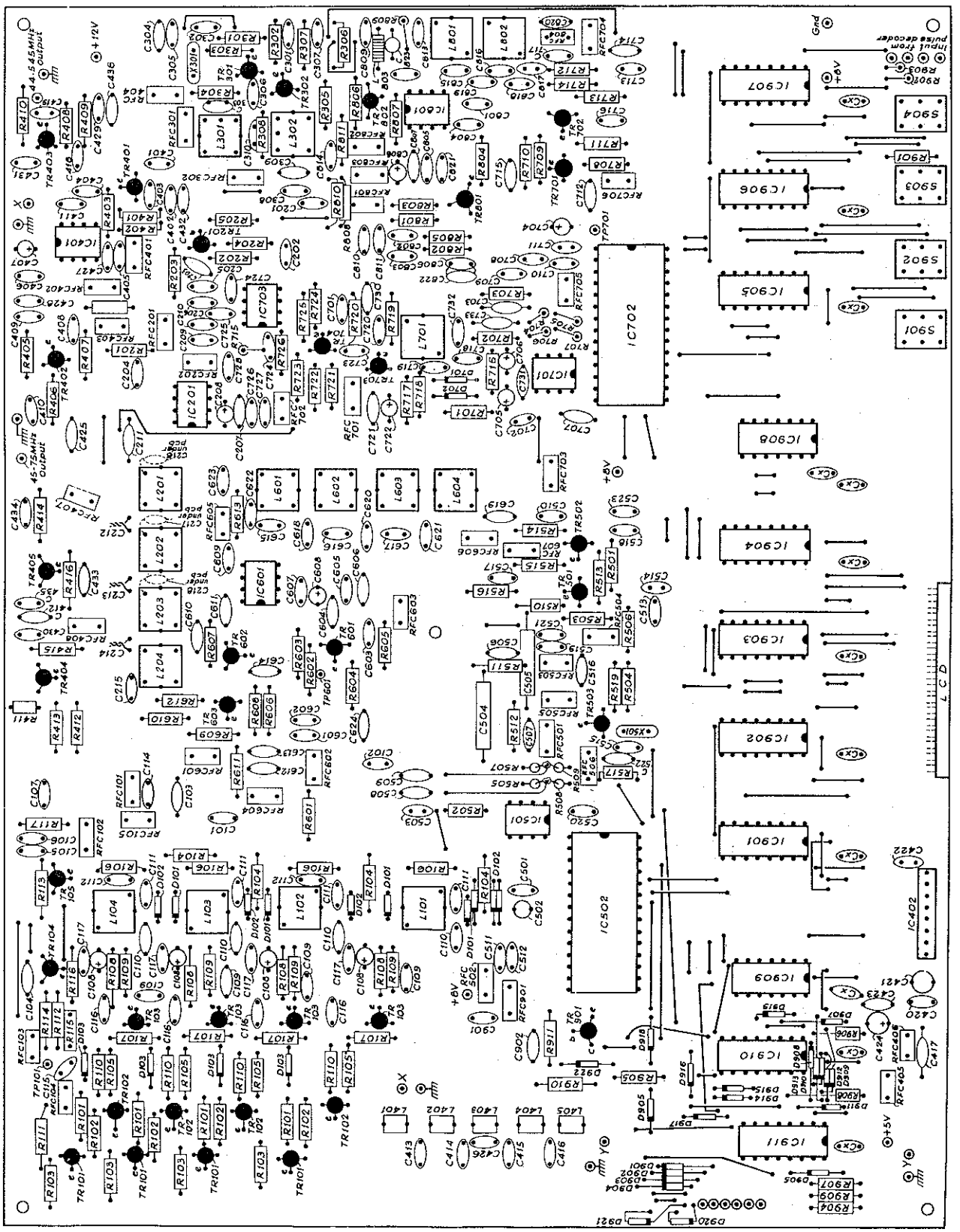

Fig 7 Main pcb component layout

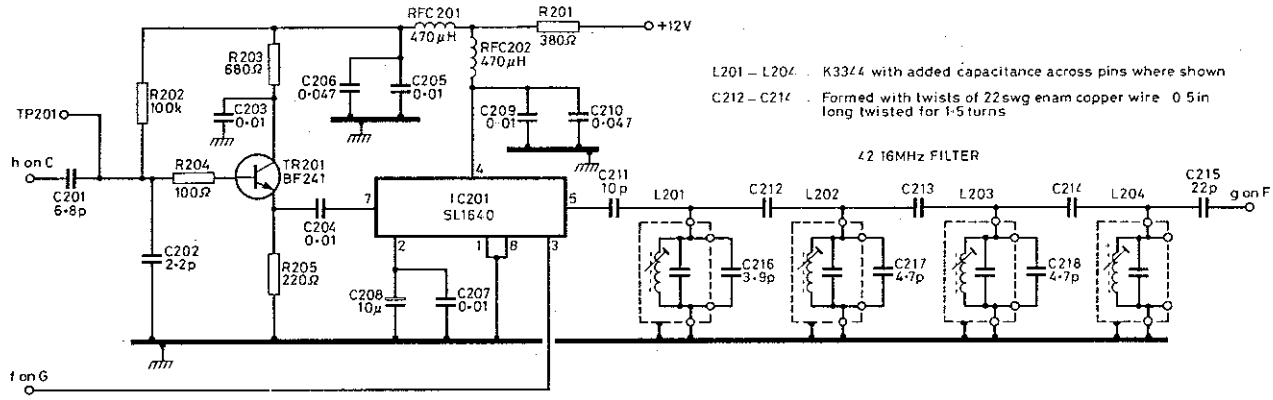

Fig 8. Section B. Second mixer and 42MHz filter

The varicap diodes are BB109B, with additional ITT210 diodes in parallel with the BB109B in the lowest frequency vco to provide for the required range of capacitance. Other diodes would be suitable, but these gave the best results of those which were tried.

The four vcos occupy the top left-hand side of the pcb with the buffer amplifier, which is common to all four, just above them. The layout can be seen in Fig 7, which shows the board viewed from the component side.

The section should be assembled and tested on the board by providing 12V at the emitters of the four TR102, and switching on each oscillator in turn by applying a volt or two at the appropriate R103. Each oscillator should be tuned to run somewhere at the bottom end of its appointed range.

Section B. Second mixer and 42MHz filter (Fig 8)

The mixer IC here, like the other three in the system, is an SL1640. Note the double-decoupling capacitors. R201 drops the 12V line to 6V. Pin 3 on IC201 is fed from the divide-by-forty IC in section G; the frequency at this point should be between 2·38469 and 2·39108MHz and at approximately 100mV. Pin 7 is fed from the 44·545MHz crystal oscillator (section C) via TR201, a BF241. The output at pin 5 is taken to the 42MHz filter via C211. Note that the capacitors C216–218 are small ceramic chips soldered across the pins of the inductances L201–203. The latter are all Toko K3344. C212–214 are small capacitances, made by twisting 0·5in lengths of 22g enamelled copper wire, 1·5 turns.

Section C. 44·545MHz crystal oscillator (Fig 9)

This section is a straight-forward crystal oscillator at 44·545MHz followed by a tuned buffer amplifier. Both L301 and L302 are K3335 from Toko, but the small winding is not used in L301. The section is sited near the top right-hand side of the board. Once it has been assembled it can be tested for oscillation at the required frequency, and the cores are adjusted for the best ouput. The frequency can be "pulled" to that which is needed by altering the value of C302.

R8 across L302 is to dampen out spurious oscillation

Section D. Output buffers (Fig 10)

This section provides output buffers for the first two injections to the main board of the receiver, and provides for a frequency read-out.

The input to TR401 and TR403, marked j on Fig 10, is from the 44·545MHz oscillator in section C. IC401 mixes this with the vco output loop 1, which has been filtered and buffered by TR404, TR405 and associated circuitry, and applied to pin 3 of IC401 (another SL1640) via its buffer TR402. The difference frequency at the output pin 5 is filtered by the lowpass filter L401, 402, 403, 404 etc and divided by 10, in IC402, before being displayed in the FC177. The latter is an lcd module with internal arrangements, which can be programmed to apply the 455kHz offset, so that the display is that of the receiver frequency.

The lowpass filter is designed to give the steadiest read-out on the lcd. It should cut-off sharply above 30MHz. There is a pin on the board at the co-axial connection to C411 on the output of IC401. The TR403 buffer, which includes an output pin on the board for the co-axial lead to the second injection point on the receiver, is sited in the top right-hand corner of the pcb, with the other buffers and mixer (IC401) to the left of it. All the rfcs on this section, like most of the others in the synthesizer are Toko 7BS series.

The display (an FC177 module from Cirkit) is mounted on the very edge of the board. 20mm lengths of 20g copper wire are soldered to the tracks on the board projecting forwards over the edge, these are slipped through the holes in the sixteen connections of the lcd and soldered. The wires are then trimmed off. The IC402 (HD10551) is mounted just to the left.

Section E. First loop, phase discriminator (Fig 11)

IC502 is the MC145151. Pin 1 is the input to the main divider, the count of which is programmed by pins 11 to 25, excluding 21. These pins are high unless grounded. In this synthesizer, their state is controlled by the output data on the 74C193 chain in section J. There is a further divider in the MC145151, which is programmed by the state of pins 5, 6 and 7. This

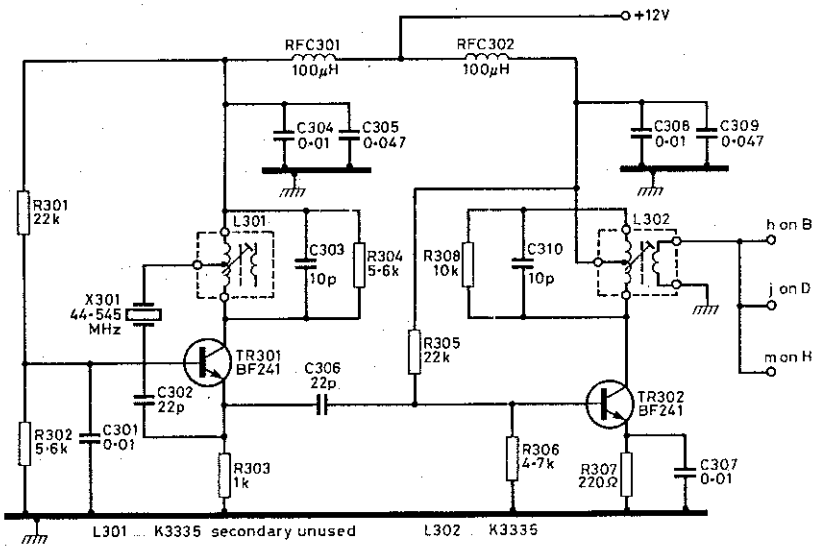

Fig 9. Section C 44·545MHz oscillator

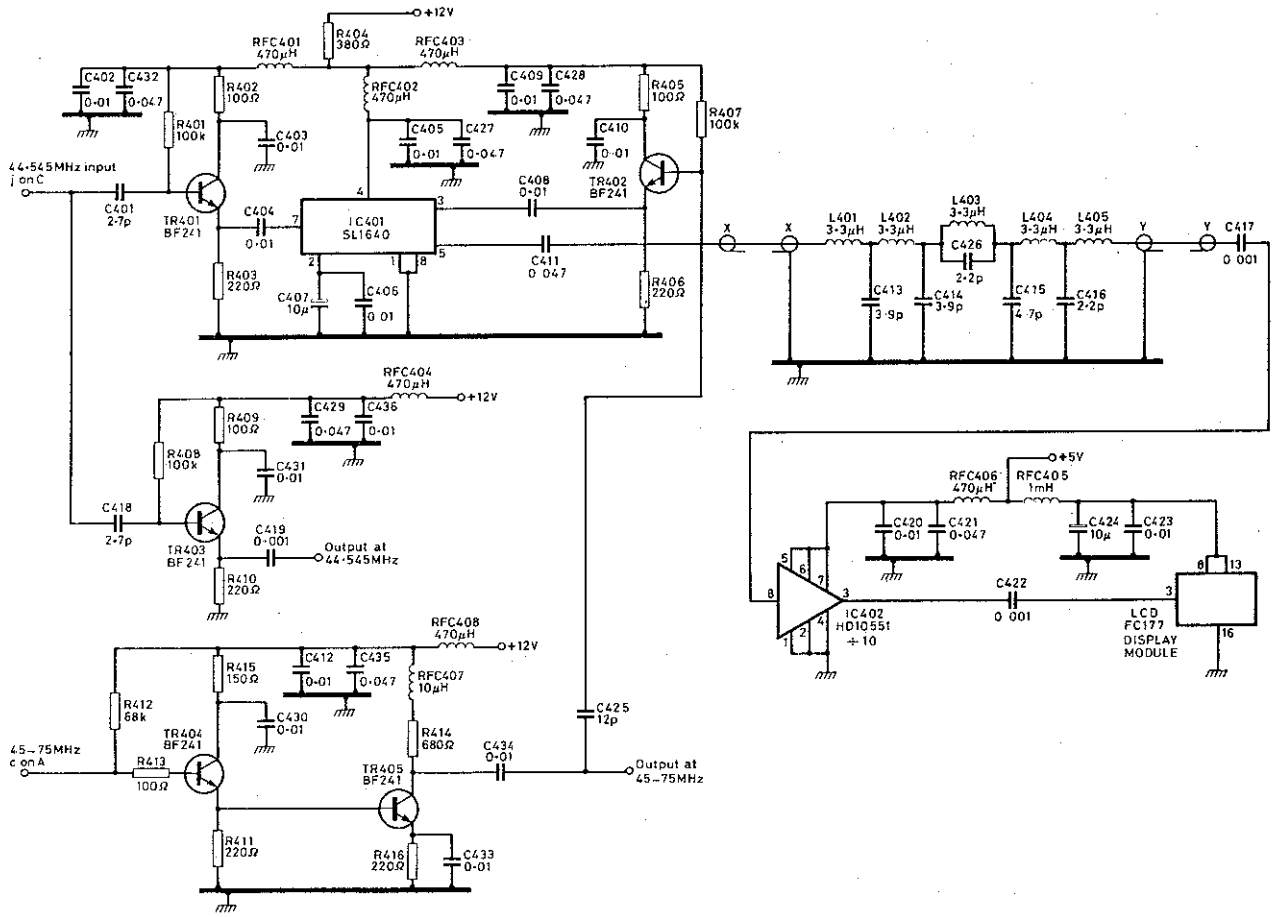

Fig 10 Section D. Output buffers and display circuit

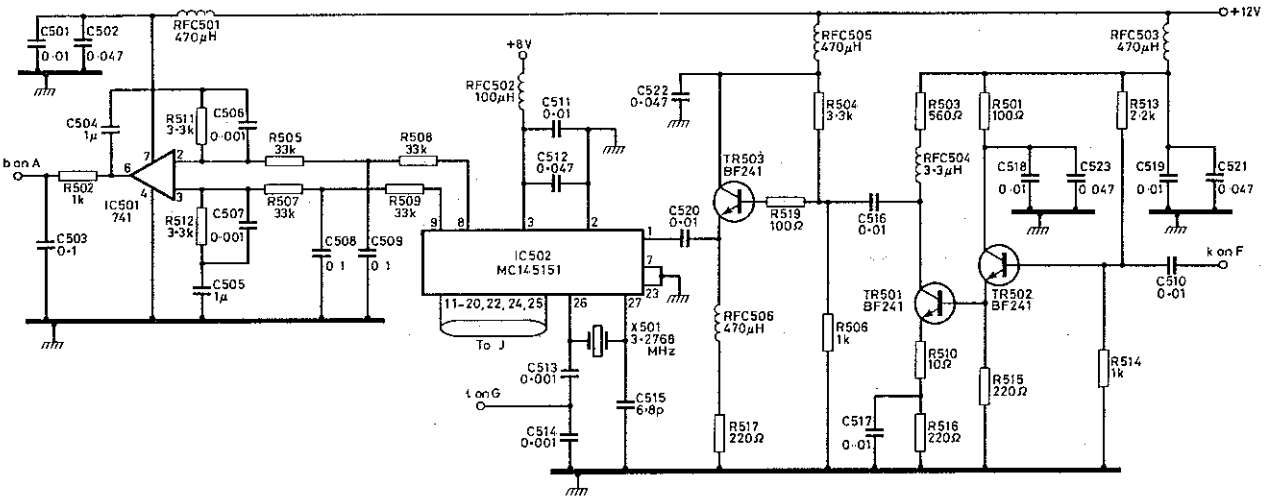

Fig 11 Section E. First loop phase discriminator and lpf

divider sets the reference frequency. There is also an internal oscillator, the frequency of which is set by a crystal between pins 26 and 27. In this case, the frequency is 3·2768MHz, and pin 7 is grounded to give an internal division by 512, making the reference frequency 6·4kHz. C513 and 514 on pin 26 allow the 3·2768MHz to be used by the other similar device on the board. C515 pulls the crystal onto the correct frequency. This may need alteration.

Any discrepancy between the input frequency after division and the reference frequency of 6·4kHz, results in a push-pull output at pins 8 and 9. This drives the IC501, a 741 op-amp, which is arranged as a lowpass filter. The output from pin 6 of IC501 controls the frequency of the vco

TO BE CONTINUED