DIRECT DIGITAL SYNTHESIS — DDS

Recent developments in integrated circuit technology have made it possible to build all-digital frequency synthesizers. Following a short remedial course on traditional synthesizer circuits, this article looks at the operation of DDS, its advantages and disadvantages.

by Dipl. Ing. G. Kleine

PLL and synthesizer circuits

SYNTHESIZER circuits are used to generate AF and RF signals with a stable frequency. They are usually based on a phase-locked loop (PLL) circuit as illustrated in Fig. 1. The output frequency is supplied by a VCO (voltage-controlled oscillator). A phase detector compares the frequency (or the phase) of the VCO output signal with a reference frequency f_{ref}. The output signal of the phase detector is an error signal that is filtered before it is applied to the VCO as a control voltage. When the PLL is locked, the VCO is phase-locked to the frequency reference.

Since it is usually required for the VCO to cover a certain frequency range or channel raster, the basic PLL is extended with a programmable frequency divider. This results in a simple frequency synthesizer circuit (Fig. 2). The VCO allowing every frequency between f_{ref} and $N_{max} \cdot f_{ref}$ can be generated by appropriate setting of the programmable divider, N. The factor N_{max} is the maximum divide ratio that can be set on the divider. Provided the loop filter is correctly dimensioned, the stability of the output frequency equals that of the reference frequency.

Where relatively high output frequencies are required (say, >100 MHz) a fast prescaler (÷N) is used ahead of the programmable divider (÷N). Since the use of a prescaler increases the step size of the synthesizer from f_{ref} to $N \cdot f_{ref}$, the reference frequency may have to be lowered to achieve the same channel raster.

The drawbacks normally associated with a low reference frequency are negated by a modulo-2 prescaler, whose scaling factor can be switched between N and $N+1$. Figure 3 shows the block diagram of a such a synthesizer. The counters 'A' and 'M' are clocked by the output signal of the prescaler, and count up to a preset value. Counter 'A' determines the rate at which the prescaler divides by $N+1$. On reaching its preset (end) value, it switches the prescaler to scaling factor N. The prescaler then divides by N until counter 'M' also reaches its preset (end) value. When this happens, counter 'M' resets itself as well as counter 'A', and the prescaler is switched back to division by $N+1$.

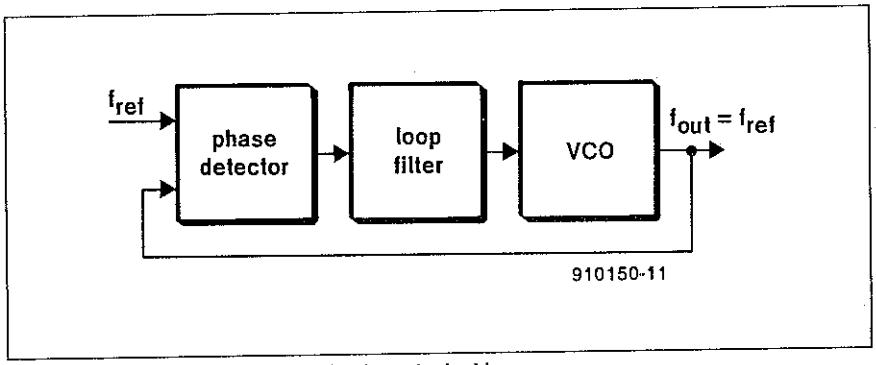

Fig. 1. Block diagram of a classic phase-locked loop.

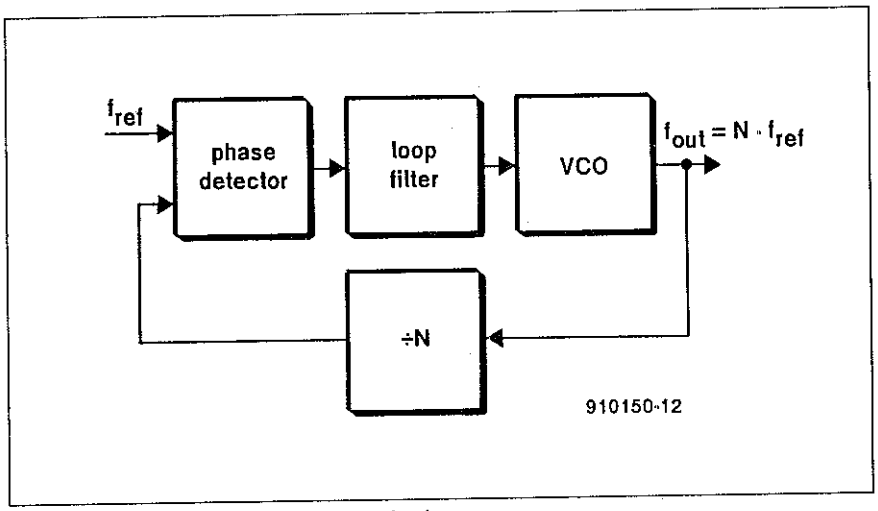

Fig. 2. Block diagram of a simple synthesizer.

It will be clear that the modulo-2 principle works only when M is greater than A. The two counters give rise to a time-averaged scaling factor, P, which is calculated from

$$P = (N+1)\ A + N\ (M-A)$$
$$P = N\ M + A$$

The modulo-2 principle thus allows channel rasters with frequency steps of f_{ref} to be achieved at relatively high frequencies. As an example, consider a synthesizer with a ÷10/÷11 prescaler (i.e. N=10). A=0 to 9, M=10, 11, 12, etc. This results in P=10 M+A, so that all scaling factors starting with 100 can be used without 'gaps'.

A disadvantage of the synthesizer circuits discussed so far is that the output frequency is invariably a multiple of f_{ref}. This can be overcome by the so-called fractional-n system (Fig. 4). As in the modulo-2 system, scaling factors are switched, which results in an average scaling factor that is not an integer (e.g., 145.23). This is achieved with the aid of an accumulator.

whose contents are incremented by F on every clock pulse. When the value L is reached the accumulator switches the prescaler to division by $N+1$ during one clock pulse. The number of clock pulses over and above L remain in the accumulator as the new start value. It can be shown that this system gives rise to an average scaling factor

$$P = N + F/L$$

This means that every required frequency resolution of the synthesizer can be achieved by appropriate choice of N and L. As an example consider a system in which N=10, F=0 to 9, and L=10. Hence, P=10+F/10, so that scaling factors such as 10.1, 10.2, etc. to 10.9 can be set via the increment F.

An extensive discussion of the operation and design of the PLL and synthesizer circuits discussed above may be found in Ref. 1. This background literature also provides a type classification of PLL circuits and phase detector circuits. In addition, an overview is given of available PLL and synthesizer ICs.

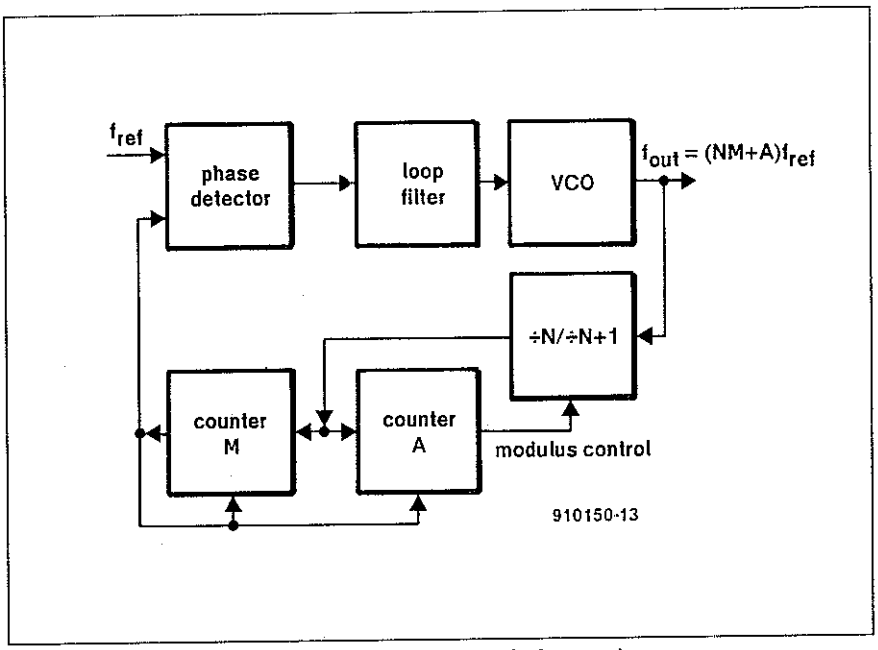

Fig. 3 Block diagram of a synthesizer with a modulo-2 prescaler.

Direct digital synthesis — DDS

A new, all-digital way of generating AF and RF signals is offered by DDS. The principle is shown in Fig. 5. A phase increment register with high resolution (e.g., L=32 bits) is provided with a value F that corresponds to the rate at which the phase of the clock signal f_{clk} is changed. Next, F is added to the existing phase value stored in a latch, and the result ends up in the latch again. When an overflow occurs in the adder the L-bit-wide result is stored in the latch. This means that there is no carry on position L+1. The phase value held in the latch forms the address for a sine function ROM, whose data are applied to a D-A (digital-to-analogue) converter. As with

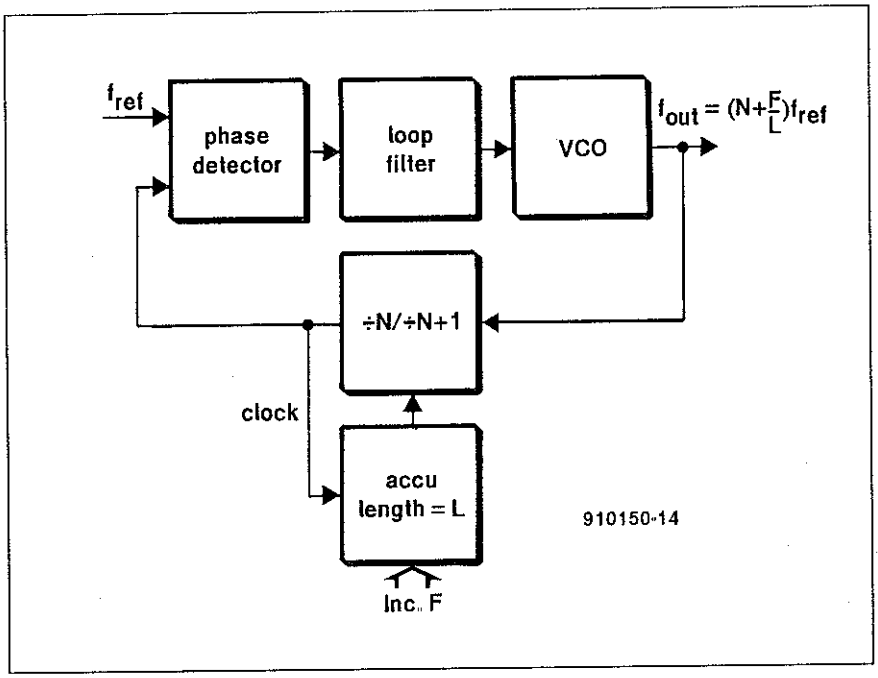

Fig. 4. Block diagram of a fractional-n synthesizer.

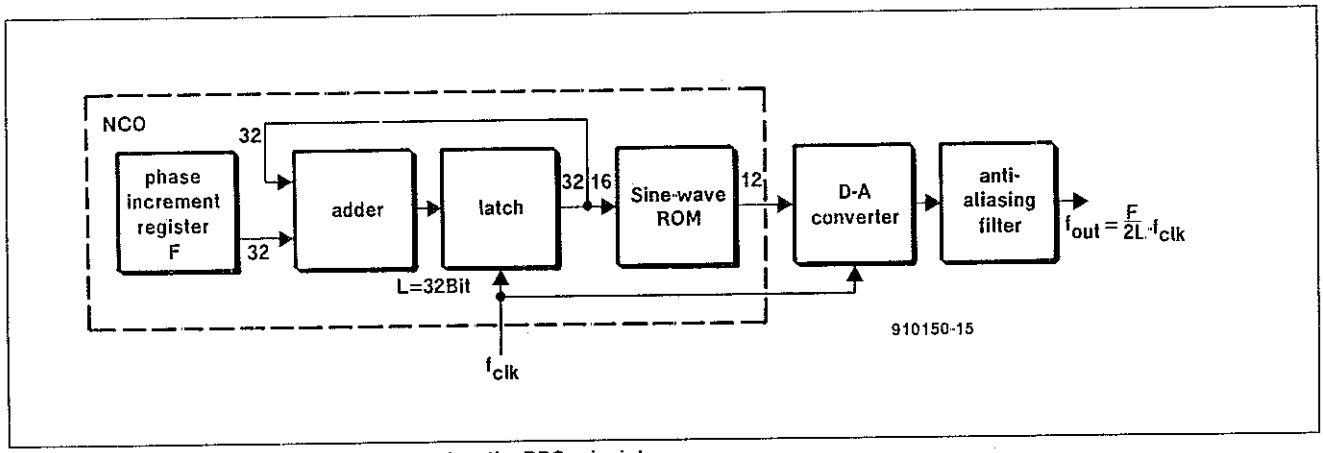

Fig. 5. Block diagram of a synthesizer based on the DDS principle.

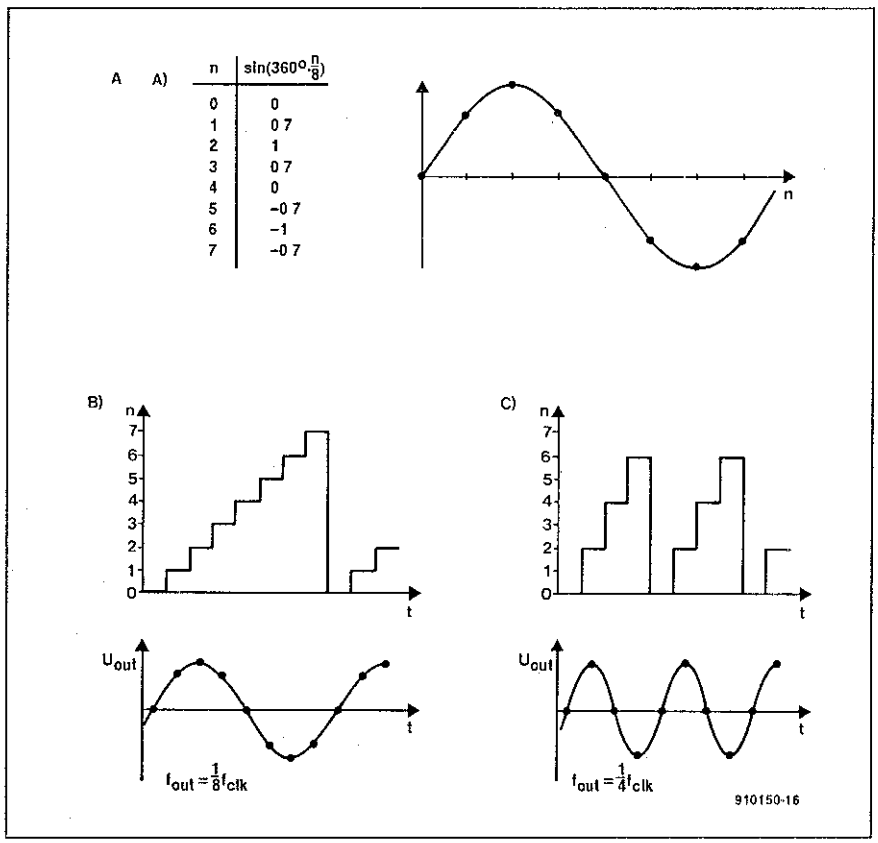

Fig. 6 (a) Contents of the sine function ROM at a resolution of 3 bits. (b) Waveform generated with a phase increment of 1×360°/8. (c) Ditto for 2×360°/8.

any other sampling system, this D-A conversion must be followed by an anti-aliasing filter that serves to suppress spectral components above $f_{clk}/2$

The power of DDS arises mainly from the high resolution of the phase increment register, the adder and the latch. In Fig. 5, for example, the resolution is represented by L, which has a width of 32 bits. The full resolution need not be used throughout the system, however. The sine function ROM is addressed by, for instance, the most-significant 16 bits of L, while the resolution of the DAC is still lower at 12 bits.

In theory, the maximum output frequency of a DDS-based synthesizer is $\frac{1}{2}f_{clk}$. In practice, however, values of $0.2f_{clk}$ to $0.4f_{clk}$ are achieved because of the anti-aliasing filter (see Fig. 7a). The phase increment, F, and the phase resolution, L, determine the output frequency, f_o, of the DD synthesizer:

$$f_o = (F / 2^L) \cdot f_{clk}$$

where a frequency resolution of

$$f_{clk} / 2^L$$

is achieved. As an example, consider a DDS in which f_{clk}=100 MHz and L=32 bits. This offers an impressive resolution of 0.0233 Hz at f_o.

The operation of the sine function ROM is illustrated in Fig. 6. Figure 6a shows the output values of the ROM at a resolution of 3 bits. One period of the sine function consists of 8 discrete steps (n=0 to 7), of which the corresponding values are stored in digital form at address n. Figure 6b shows the value of n in the latch output signal for a phase increment, F, of 1. Shown below is the signal after the D-A converter and the anti-aliasing filter. The amplitude values of this signal correspond to the entries in the sine function ROM table (Fig. 6a). The output frequency, f_o, equals $\frac{1}{8}f_{clk}$.

The effect of increasing the phase increment, F, to 2 is shown in Fig. 6c. It is seen that the range of phase values (or ROM addresses), n, is cycled through twice as fast, which results in f_o doubling to $\frac{1}{4}f_{clk}$.

The output frequency spectrum of a DD synthesizer will inevitably contain certain spurious components (Fig. 7). A number of these are alias components caused by the sampling operation (Fig. 7a). These components occur at

$$f_{+alias}(i) = i \cdot f_{clk} + f_o$$

and at

$$f_{-alias}(i) = i \cdot f_{clk} - f_o$$

where i is 1, 2, 3, . . . The component written as $f_{-alias}(1) = f_{clk} - f_o$ is the critical component for the anti-aliasing filter. Figure 7a shows this for a DDS in which f_o=15 MHz and f_{clk}=40 MHz.

The other spurious components in the output spectrum are caused by the limited resolution and non-linearity (quantization errors etc.) of the D-A converter. These components are multiples of the output frequency as well as intermodulation products caused by 'imaging' with the y-axis and the component $f_{clk}/2$. Fig. 7b shows these additional spurious products at f_o=15 MHz and f_{clk}=40 MHz. A number of components formed by imaging with f=0 and $f=f_{clk}/2$ are indicated.

The level of the alias components depends directly on the resolution of the D-A converter whose non-linearity in addition determines the level of the other spurious components. As in any other real-time sampling system, the alias components are $(\sin x)/x$ weighted (Fig. 7a), so that their level drops with increasing frequency.

The digital circuit between the phase increment resister and the sine function ROM is usually referred to as an NCO (numerically controlled oscillator) (Refs. 2; 3). A number of currently available DDS ICs have an on-board DAC—others require an external DAC. Where the address lines of the ROM are accessible, a different conversion table may be used to implement other waveforms, e.g. a triangular wave. There exist also DDS ICs that contain a sine and a cosine function in ROM. These ICs enable two output signals with a phase difference of exactly 90° to be generated. Such signals are often required as carriers representing I- (in phase) and Q (quadrature) components in complex modulator circuits (Refs. 2; 4; 5).

The output signal may be modulated by extending the block diagram in Fig. 5. Inserting an adder stage between the latch and the sine function ROM enables either phase modulation (PM, PSK, BPSK, QPSK) or frequency modulation (FM, FSK) to be realized by adding phase values. Similarly amplitude modulation (double-sideband AM with carrier) is achieved by inserting a multiplier between the sine function ROM and the DAC. Since all three modulation systems are implemented with digital means, they are in principle purely linear. More information on analogue and digital modulation systems may be found in Ref. 4.

DDS: outlook

Although DDS components are still relatively expensive, they have some advantages that give them a potential for wide practical use. In addition to the high resol-

ution of the output frequency the short lock (settling) time is particularly valued By contrast, traditional synthesizers have a loop filter whose response to the VCO control voltage slows down the speed at which the synthesizer can change its output frequency

As already mentioned, DDS offers the possibility of pure linear modulation of the output signal. It should be noted however, that the all-digital modulation causes certain spurious products in the output signal. The level of these products can be reduced by increasing the resolution of the phase increment register and the D-A converter

A further advantage of a DD synthesizer is its wide output frequency range of several decades. Again by contrast this is almost impossible to achieve with traditional VCOs. Finally, the stability of the output frequency depends on the reference clock f_{clk} only This means that ageing effects in the clock source are ruled out thanks to the all-digital principle of operation ■

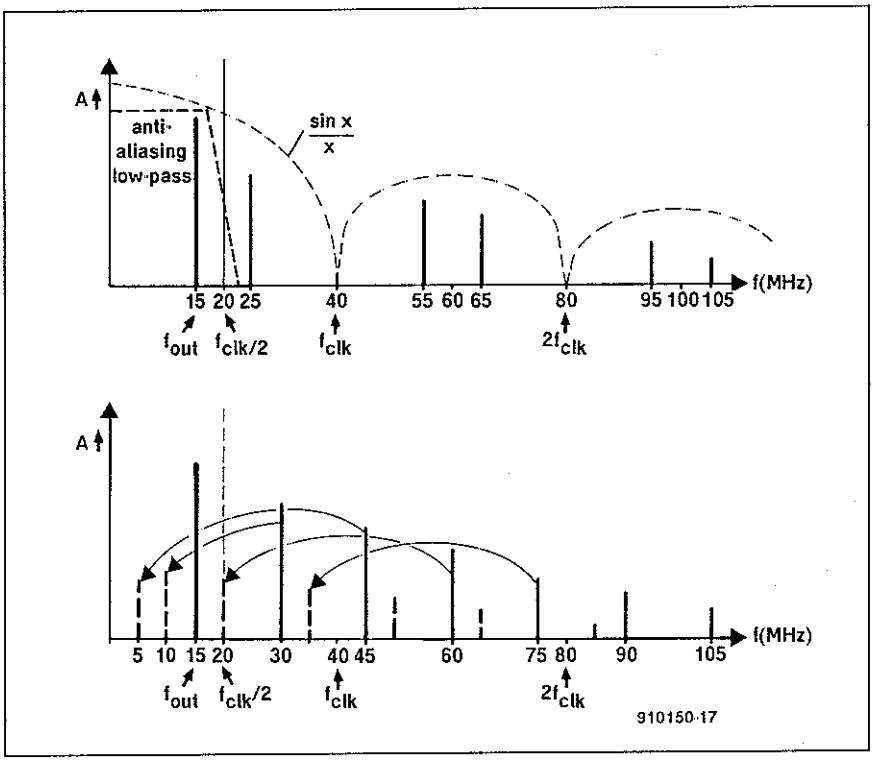

Fig. 7. Alias and spurious components in a DDS spectrum. The solid vertical lines represent multiples of f_{out}. The dashed vertical lines represent image products relative to f=0 or $f_{clk}/2$

References:

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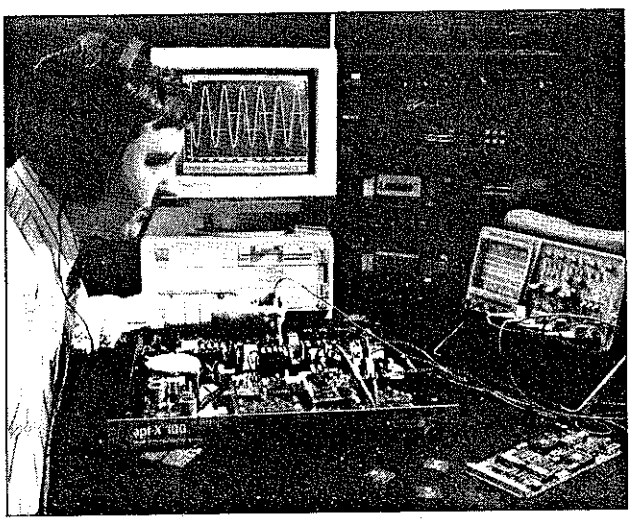
2. The DDS Handbook (second edition) Published by Stanford Telecom *
3. Design notes published by Rohde & Schwarz Stanford Telecom/Alfatron GmbH, Plessey, Tricom Mikrowellen GmbH, Qualcomm Inc.
4a. Analoge Modulationsverfahren (Analogue modulation systems) By R Mäusl Published by Hüthig Verlag
4b. Digitale Modulationsverfahren (Digital modulation systems). By R Mäusl Published by Hüthig Verlag.
5. Audio spectrum shift techniques *Elektor Electronics* October 1991

* This book may be ordered from Alfatron GmbH, Stahlgruberring 12, 8000 München 82, Germany. Telephone: +49 89 420491-0 Fax: +49 89 420491-59

AN INNOVATIVE MUSIC COMPRESSION SYSTEM

Dr Ian Mack, a researcher in the Department of Electrical and Electronic Engineering Queen's University, Belfast, Northern Ireland, is seen evaluating the noise performance of the APT-X 100 digital audio data compression system, which was developed by Audio Processing Technology. It is thought to be the first of its kind in the world which quadruples the supply of digital music signals stored on a compact disc.



The brains of the system are the high-speed digital signal processor (DSP) chips, shown in the foreground, to code and compress from 16 to four, the binary digits (bits) which represent the audio signals with no loss of quality

The breakthrough not only has far-reaching implications for the music industry, but also in the field of satellite communications Since it would mean the reduction to a quarter of the current number of sound signals transmitted by satellite, it would reduce to a quarter the bill for expensive satellite time.

The company was founded jointly in 1988 by Stephen Smyth as a result of research undertaken by him while he was a student at Queen's University, and QUBIS, a holding company of the university, that provided the initial funding. In 1989, Solid State of Oxford became the majority shareholder.

For further information, contact

Paul Smith, Publicity Coordinator, Audio Processing Technology Ltd , 21 Stranmillis Road, Belfast, Northern Ireland BT9 5AF Telephone: (0232) 662714 Fax: (0232) 382208.