One c-mos gate pack can form the heart of a frequency meter, a step-down switching regulator or a negative-supply generator, explains Rae Perälä.

Gates open up

There are many applications for the 4011 c-mos two-input-nand gate – other than just gating. This article presents three such circuits, namely a step-down regulator, a negative-voltage switching regulator, and a frequency measuring circuit

Step-down regulator

Operating principle of a typical step-down regulator is shown in **Fig. 1** Semiconductor switch S_1 is usually controlled by a pulse width modulator, or pwm.

While the switch is on, current flows through inductor *L* to the output. Simultaneously, magnetic energy in the inductor increases. Diode *D* stays in its reverse state. When the switch turns off, the inductor discharges its magnetic energy giving a current to the output. Diode D now becomes forward biased, providing path for current flow.

The on-to-off time ratio of the switch is controlled by the pwm circuit. This circuit compares output voltage, V_{out}, to reference voltage V_{ref} and changes the on-to-off ratio accordingly.

Figure 2 is a practical step-down circuit using 4011. It makes a new regulated output voltage V_{out} from a regulated +8 to +15V input voltage. Gates A and B work as an oscillator giving an asymmetrical 40kHz square wave, **Fig. 3** Gate C controls the switching transistor, which is a BS250 p-type enhancement mode mosfet This same gate inverts the oscillator output voltage, presenting the transistor control voltage V_{GS} as in Fig 3. The control voltage has long negative pulses interspersed with short intervals. The transistor conducts during the negative pulses

Gate D regulates the output voltage Its output is high when V_{out} is beneath the adjusted value. The high state activates gate C, which can now control the switching transistor. When the adjusted output voltage is reached, gate D output goes low, stopping gate C, which remains in the high state. The switching transistor has no control voltage and remains off.

The regulating circuit operates using the 'missing pulse' principle It provides pulses when the output voltage is low and ceases pulsing when the output voltage is sufficiently high

Output voltage is adjusted via the 470kΩ potentiometer. Usable output voltage range of the circuit is 0.5 to 0.9 of V_{in}. The circuit can be loaded to 100mA.

Negative voltage regulator

A negative voltage switching regulator is presented in **Fig. 4**. Gates A and B form an oscillator, giving a symmetrical square wave voltage. Gate C controls the BS250 switching transistor.

During the transistor on time, current flows through the inductor, charging the magnetic energy within it. The magnetic energy discharges while the transistor is off through the diode, producing a negative voltage at the output.

Gate C regulates the output voltage. When the output voltage is too low, the regulating input voltage of gate C is high and the oscillator voltage controls the gate C output and therefore the transistor

When the output voltage reaches the desired negative value, the regulating input goes low and it stops the output of gate C leaving it in its high state. The transistor stays off until the output voltage goes below its adjusted value.

This circuit requires an input voltage of +8V to +15V, which can be unregulated. A regulated +5V input acts as a reference voltage.

Frequency measurement on a dvm

A digital voltmeter can be used for frequency measurements to 1MHz using the circuit in **Fig. 5**. The frequency to be measured connects to the input of gate A. This input is biased with 330kΩ resistors to half the supply voltage. This allows low input voltages to change the output of gate A. **Figure 6** shows the gate voltages Output voltage of gate A changes each time the input voltage passes the half supply voltage threshold.

Gate A controls gates B and C. Gate B has a delay capacitor in its output. Figure 6 shows

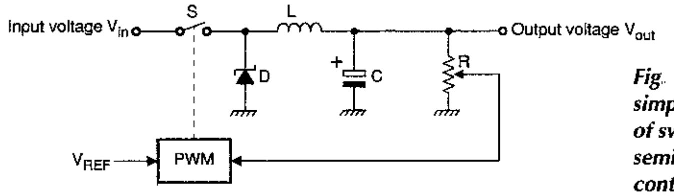

Fig. 1. Switching converter simplified. On and off times of switch S, invariably a semiconductor switch, are controlled by a pulse-width modulator.

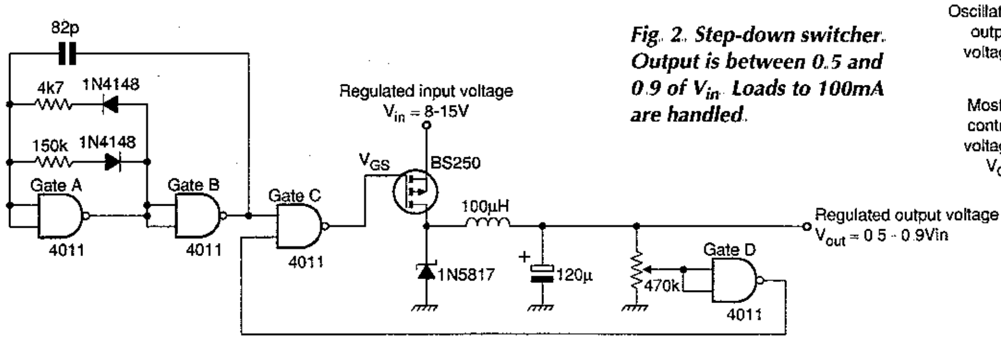

Fig. 2. Step-down switcher. Output is between 0.5 and 0.9 of V_{in}. Loads to 100mA are handled.

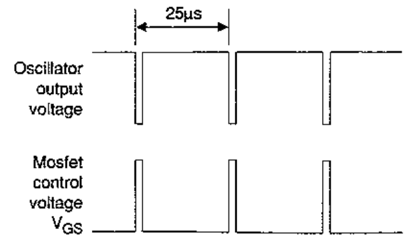

Fig. 3. Asymmetrical oscillator gates A and B of Fig. 2 runs at about 40kHz.

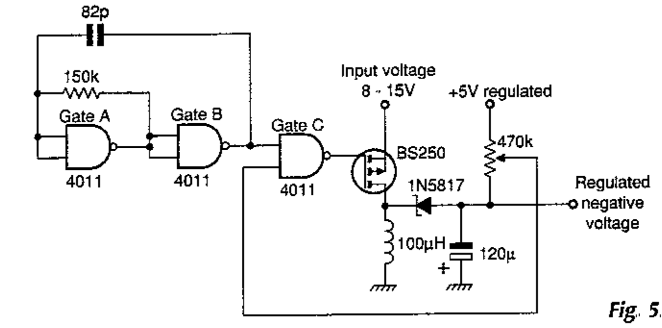

Fig. 4. Negative supply from a positive input. Again, gates A and B are an asymmetrical oscillator. Gate C determines whether drive pulses pass to the switching transistor.

with its 200mV or 2V dc voltage range selected. The meter reading can be adjusted by the 100kΩ potentiometer so that the voltage reading directly represents the unknown capacitance

Capacitance measuring ranges are selected by the switch, which connects a suitable capacitor to gate B's output. The 100pF capacitor should be a trimmer so that gate C's input capacitance can be compensated for ■

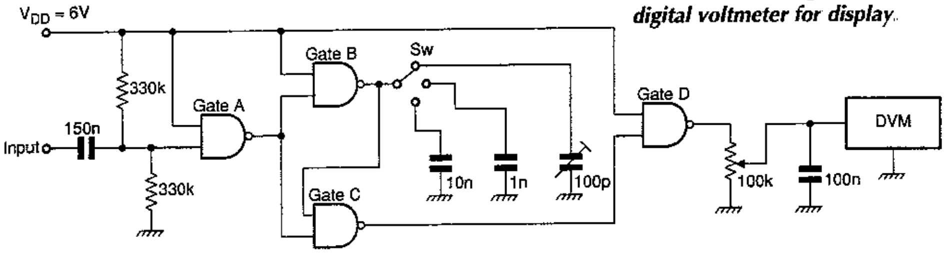

Fig. 5. Direct reading frequency meter, capable of measuring to 1MHz in three ranges, uses a digital voltmeter for display.

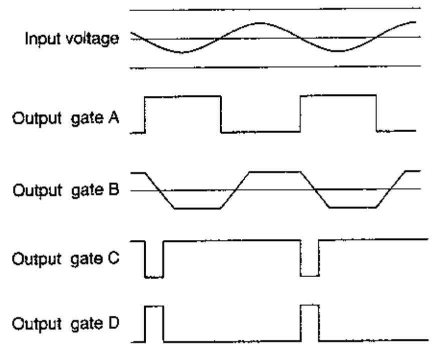

Fig. 6. Frequency meter waveforms. Top is the ac input, which is biased toward the switching point of the logic gate. In this way, the gate switches at a significantly lower input voltage than would otherwise be needed.

the gate B output voltage, which is reversed and delayed relative to gate A's output One input of gate C is fed with the output voltage of gate A and in the other input the delayed voltage from gate B. Output of gate C comprises a negative pulse with a duration equal to the the time it takes for gate B to falling from its high state to its low state. Pulses from gate B are then inverted in gate D These pulses are always similar in shape, independent of the amplitude and shape of the original input voltage.

The mean value of gate D's output voltage can then be measured by a digital voltmeter