VFO STABILIZER

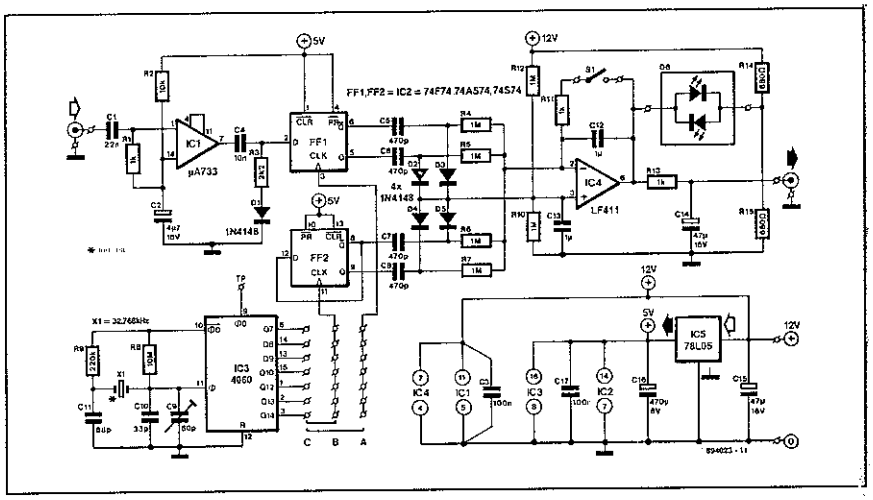
The stabilizer presented here enables the precise tuning of HF oscillators for up to 100 MHz if these have a frequency control input That input is normally used for varying the capacitance of a varactor

The signal at the input of the circuit is amplified by a fast operational amplifier, IC_1. The output of this opamp is a rectangular signal that is applied to the D (data) input of bistable FF_1 The clock input of the bistable is provided by generator IC_3 The two outputs of the bistable are the product of the clock and the input signal The frequency of this composite signal lies between 0 Hz and half the clock frequency To ensure the best possible control characteristic, the output signal of the bistable is compared with a reference signal that has a frequency one quarter of the clock To that end, a second bistable, FF_2, is connected as a binary scaler; its input is provided with a signal whose frequency is half that of the clock applied to FF_1

The differentiating network at the output of FF_1 uses only the negative pulses of the output signal, whereas that at the output of FF_2 uses only the positive pulses All these pulses are combined in an integrator, resulting in a stable control voltage Since both the Q and the $\overline{Q}$ output are used, the ripple is halved

If the frequency of the input signal is not stable, the amplitude of the integrated signal varies The variations are used to control the oscillator in a manner where the deviations are negated

The clock is constructed around a CD4060 and an inexpensive watch crystal The crystal may, of course be replaced by a different type, as long as this has the required stability



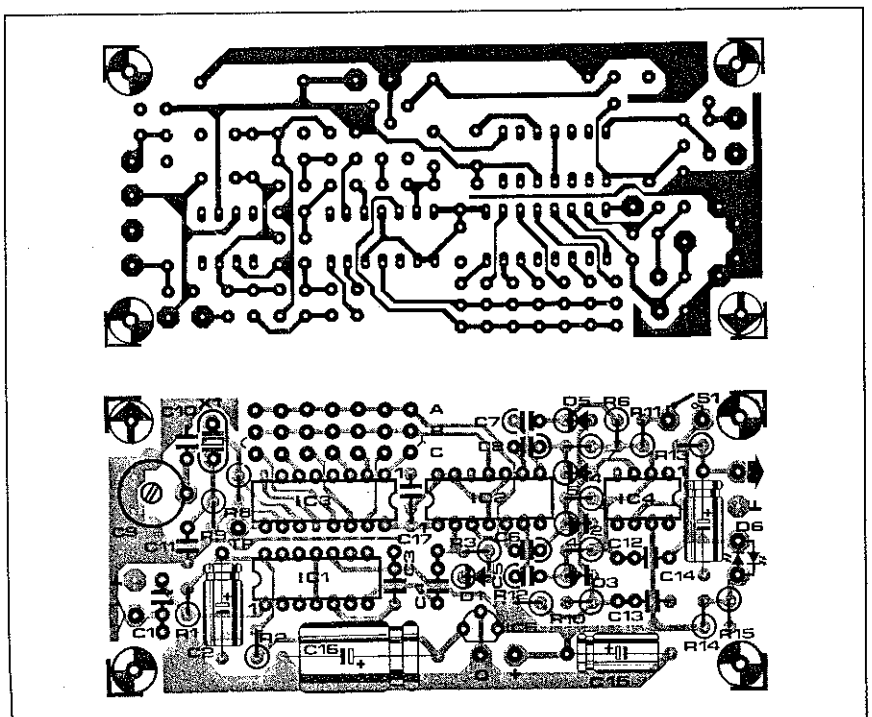
The clock frequency, and thus the required grid, is set with the aid of jump leads The frequency on row B must always be half that on row A

The construction and alignment should not present any undue problems if the circuit is built on the PCB shown below The oscillator is set to exactly its centre frequency by C_9: this can be verified at test point TP, which carries the buffered clock frequency

The circuit is powered by a 12-V supply that is brought down to 5 V and stabilized by regulator IC_5

Indicator D_6 remains out as long as long as the oscillator frequency is stable. If the frequency drifts, the LED lights, its colour and intensity indicate in what direction drift occurs and how serious the drift is

The integrating action may be disabled by S_1, which allows the circuit to settle down more rapidly than with it on ■



COMPONENTS LIST

Resistors:		
3	1k	R_1;R_{11};R_{13}
1	10k	R_2
1	2k2	R_3
6	1M0	R_4–R_7;R_{10};R_{12}
1	10M	R_8
1	220k	R_9
2	680Ω	R_{14};R_{15}
Capacitors:		
1	22n ceramic	C_1
1	4µ7 16V	C_2
1	100nF ceramic	C_3
1	10nF ceramic	C_4
4	470pF polystyrene	C_5–C_8
1	60pF trimmer	C_9
1	33pF	C_{10}
1	68pF	C_{11}
2	1µ0 MKT	C_{12};C_{13}
2	47µF 16V	C_{14};C_{15}
1	100nF MKT	C_{17}
Semiconductors:		
5	1N4148	D_1–D_5
1	bicolour LED	D_6
1	uA733	IC_1
1	74F74 or 74S74 or 74AS74	IC_2
1	CD4060	IC_3
1	LF411	IC_4
1	78L05	IC_5
Miscellaneous:		
1	SPST switch	S_1
1	crystal 32.768 kHz	X_1
1	PCB	894023