ADC-42 WINNER

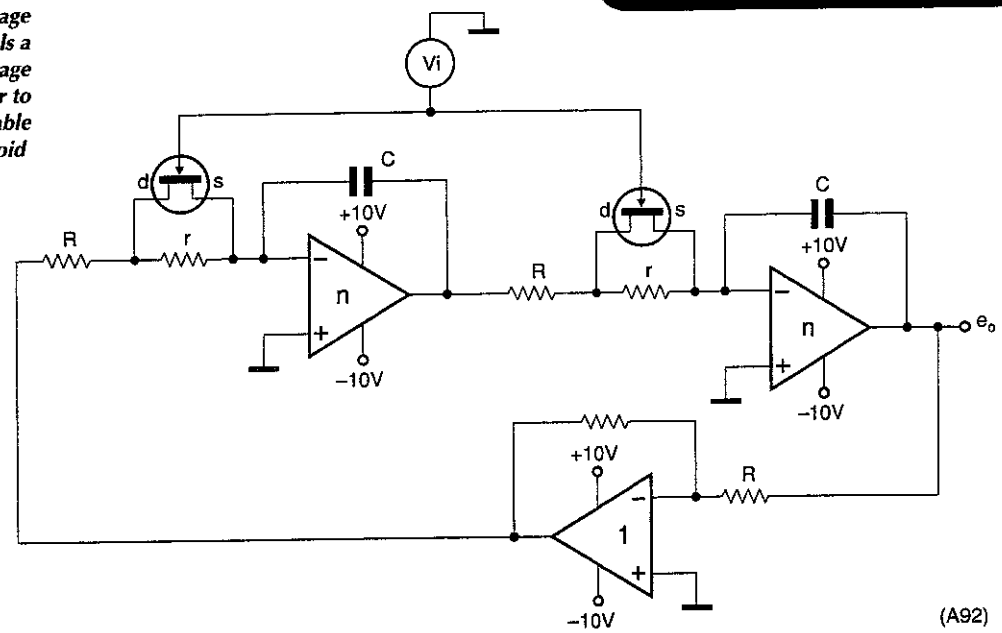

Fig 1. One voltage input controls a two-stage integrator to produce a variable sinusoid

Op-amp vco and binary fsk generator

The circuit shown can be characterised by the differential equation,

$$d^2y/dt^2+n^2y=0$$

with $y(0)=1$, the solution is $\cos nt$, which is found by the circuit and results in a sinusoidal output e_o at the frequency $f=n/(2\pi)$.

Frequency variation is obtained by varying the drain/source resistance of the two fets, thereby controlling the RC constant of each integrator, the resistive component of which is $1/(R_{eq}+R)$, R_{eq} being the parallel combination of r and the drain/source resistance $R_{ds(on)}$.

Available fets have a range of $R_{ds(on)}$ of 100Ω to 100kΩ, achieved by varying the control input V_i to each fet. Since each source is at virtual ground, the same voltage may be used with no cross loading effects.

Figure 2 shows a variation on this oscillator which performs binary frequency-shift keying. Here, the fets are replaced by analogue switches controlled by a voltage input. With the switch open, each resistive arm to the integrators is 13.257kΩ and, with the switch closed, 7.23kΩ, giving frequencies at the output of 1.2kHz and 2.2kHz. For start-up, arrange power-on switching to store 1V at C_1 and zero at C_2.

One can envisage the use of more than one switch at each op-amp to give a range of switched frequencies – three switches at each integrator would give a range of eight frequencies and twelve, perhaps controlled by a 12-bit a-to-d converter, would give 4096 frequencies.

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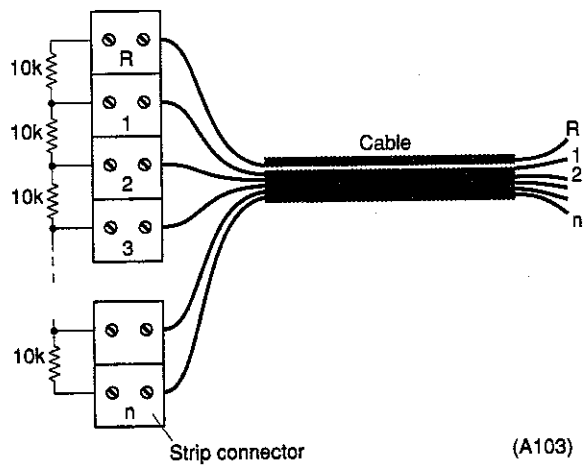
A handful of anonymous cores in a cable may be sorted out with this simple scheme and a multimeter.



Cable core identifier

A very simple arrangement of resistors allows unmarked cores in a multicore cable to be easily identified.

Connect resistors of equal value to a strip connector at the A end, as shown, with the metallic shield or an external reference to R. At the B end of the cable, assuming the resistors are of 10kΩ each, a multimeter between the shield and one of the cores will read 10kΩ, which shows that it is No 1. A reading of 20kΩ shows No 2, and so on. An absence of any reading indicates an open circuit and if several readings are the same, there are shorts.

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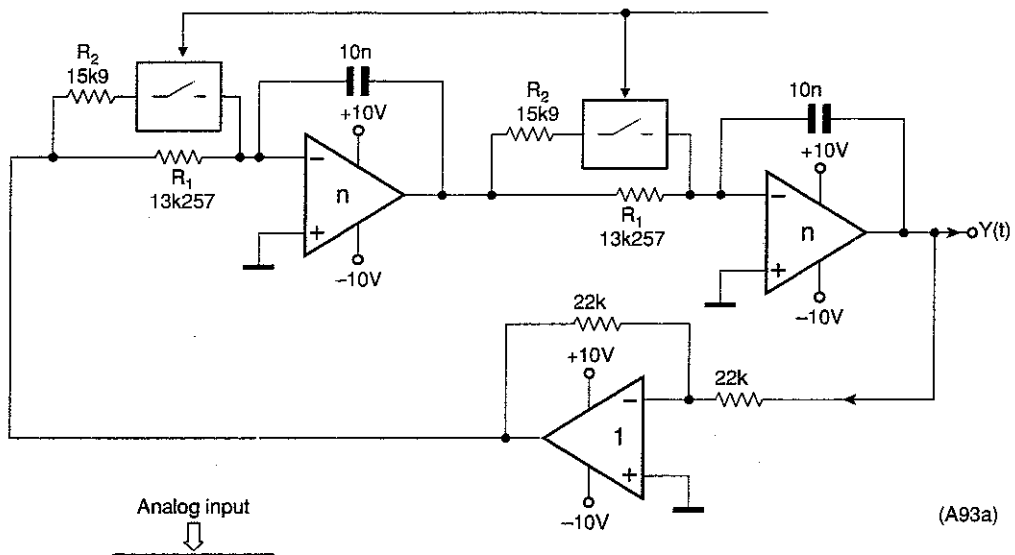
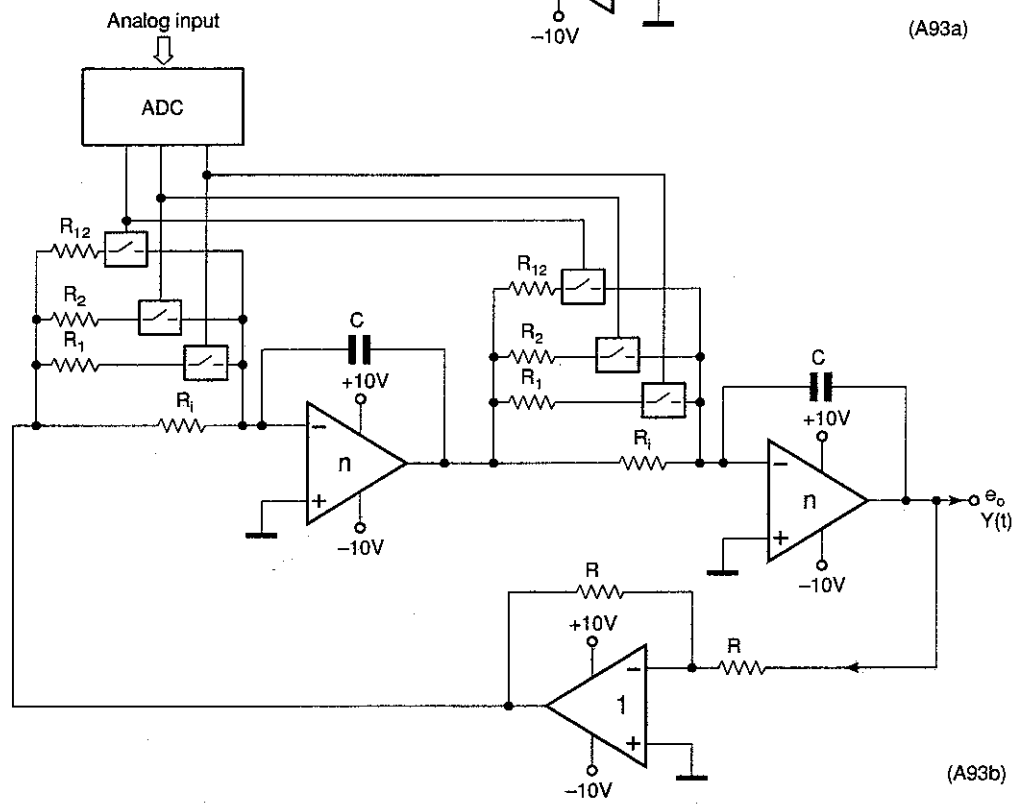


(A93a)

Fig. 2. Replacing fets by analogue switches gives a binary fsk output and the possibility of a switched-frequency generator with as many outputs as desired.



(A93b)

Improving supply rejection in cmos monostables

Using a Schmitt trigger as the output device in a cmos monostable, as in **Fig. 1**, in an effort to obtain clean transitions may cause problems with supply rejection, since threshold voltage in gates such as the *CD4093* do not scale correctly with supply voltage, so that pulse period can vary by up to 20%.

A small constant voltage in series with the timing resistor, shown in **Fig. 2**, compensates for the variation. Ideally, this would be variable to eliminate the period variation completely, but in practice, the forward voltage drop of a diode is about right; using a 4093, the variation was well-nigh perfect over the 4.5-7V range and only 3% out at 10V.

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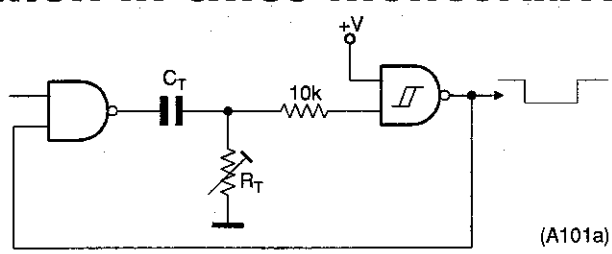
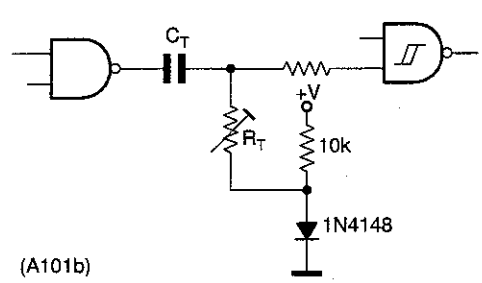


(A101a)

Fig. 1. Schmitt monostable may suffer poor supply voltage rejection



(A101b)

Fig. 2. A constant voltage, here obtained from a diode forward drop, almost completely eliminates the effect.