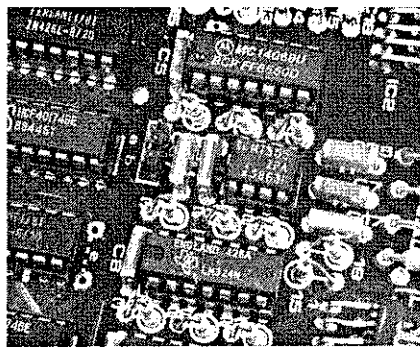


MORE APPLICATIONS FOR THE 555

There are probably few integrated circuits that have been with us for as long as timer Type 555. This article does not add to the seemingly endless list of AMV and MMV applications of this chip, but discusses some less familiar designs derived from these. In addition, a brief introduction is given to the new CMOS and LinCMOS versions of the 555.

by T. Wigmore

One explanation of the popularity of the now 17-year-old timer type 555 may be that the chip is inexpensive, and contains a fairly unique combination of sub-circuits. Looking at the internal structure shown in Fig. 1, these are a bistable (a digital circuit), two comparators (analogue circuits) and some discrete parts, a resistive potential divider and a transistor. Added to the versatility of these interesting building blocks come the abilities of the chip to supply a relatively high output current, and to work from a wide range of supply voltages. Pin assignments of the 555 and the dual version of it, the 556, are given in Fig 2. Every electronic engineer or student is bound, at some time, to deal with the 555 in its standard configuration as a monostable or astable multivibrator. These applications are so numerous by now that it is often forgotten, or not even known, that the 555 can be used in a number of other, less well known, configurations. To understand how these work, however, it is useful to first look at the basic operation of the chip.



A) and a threshold comparator, block B, are clearly recognized as difference amplifiers. The bistable, block C, is, perhaps, less conspicuous. In rest, transistors Q₁₅ and Q₁₇ are off, while Q₁₆ and Q₂₀ conduct. When the trigger voltage drops below one-third of the supply voltage, Q₁₀, Q₁₁ and, therefore, Q₁₅, also start to conduct. Transistor Q₁₅ removes the base drive of Q₁₆ and so causes this to block. By virtue of R₁₀ and diode Q₁₈, Q₁₇ starts to conduct. As the trigger voltage rises again, Q₁₅ is allowed to turn off again without causing instability of the new state — Q₁₆ is

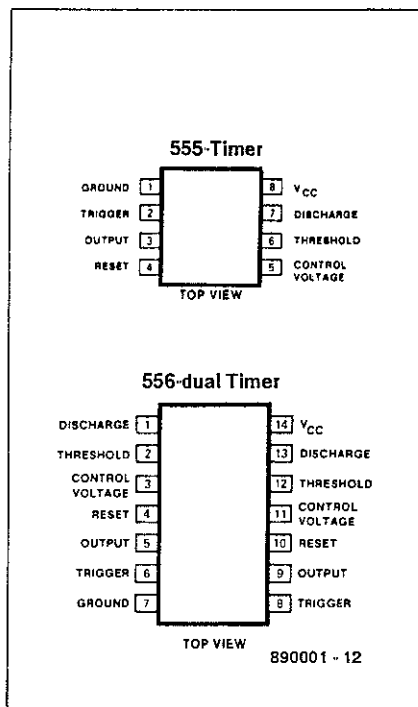


Fig. 2 Pinning of the 555 and the 556

Some fundamentals

Judging from the internal diagram of the 555 (Fig. 3), the relatively high number of components is typical of chip technology of the early 1970s. Fortunately, the internal diagram is still fairly simple to analyse. A trigger comparator (block

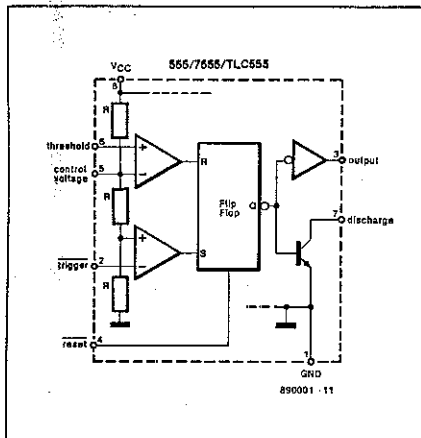


Fig. 1. Basic internal structure of the 555.

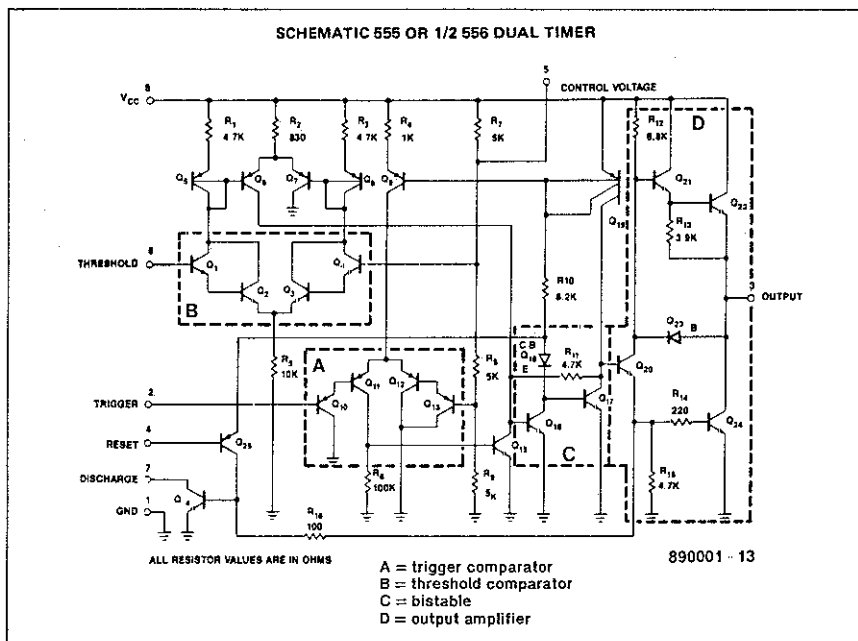


Fig. 3 Detailed internal circuit diagram of the 555.

Fig.

a

b

Fig. curr lower dec The anno

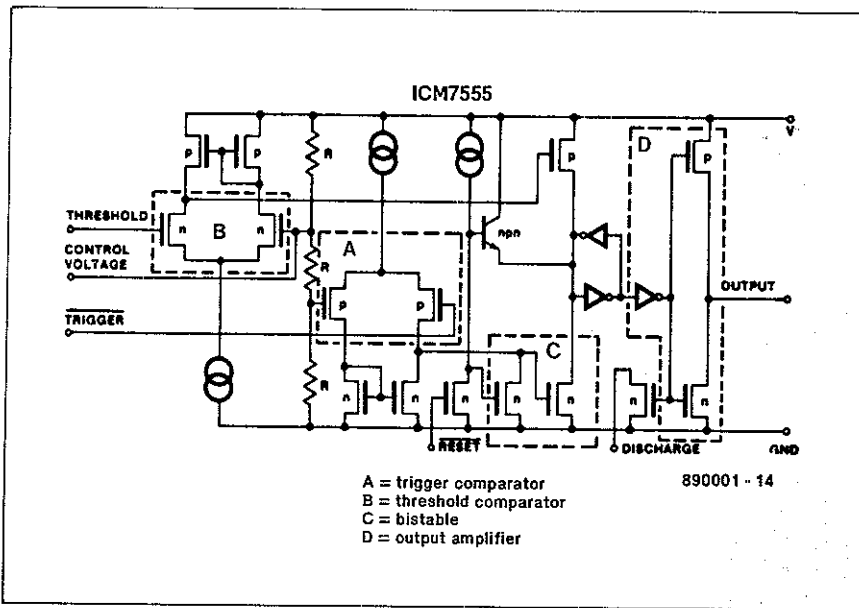


Fig. 4. Internal structure of a CMOS version of the 555, the ICM7555 from Intersil.

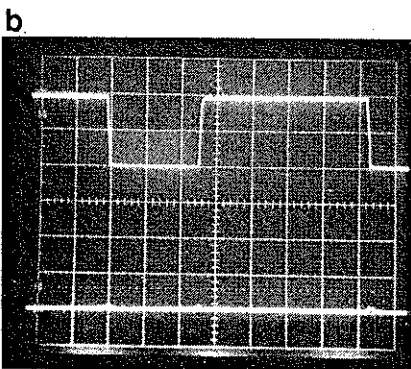
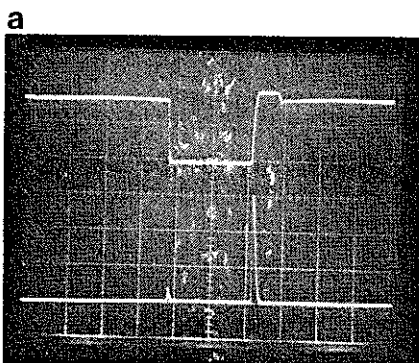


Fig. 5. A standard 555 briefly draws a high current when its output toggles (Fig 5a; lower trace shows inverted supply voltage; decoupling of the supply voltage is a must!). The new CMOS 555 does not produce this annoying effect (Fig. 5b)

then inhibited from conducting via R_{11} . The normal procedure is that the threshold voltage exceeds two-thirds of the supply voltage. This results in Q_1 and Q_2 starting to conduct. The increase in their collector currents is amplified by Q_5 and Q_6 , so that Q_{16} starts to conduct again. This transistor, in turn, causes Q_{17} to block, but only if Q_{15} is actually off. If this is not so — in other words, if the threshold input and the trigger input are both actuated — the bistable remains reset. Because the collector current of Q_6 is limited by R_2 , Q_{15} pulls the base of Q_{16} harder to ground than Q_6 can pull it to the positive supply rail.

An all-overriding method to reset the bistable is to drive its reset input low. This results in Q_{25} conducting, so that the base drive of Q_{17} is removed. Since diode Q_{18} creates additional voltage drop during resetting, the base voltage of Q_{17} is sufficiently low to actually turn this transistor off. When the bistable is in the reset state, output transistors Q_{20} and Q_{24} and, via R_{16} , discharge transistor Q_{14} , conduct.

The 555 briefly draws a fairly high current when its output changes from low to high. This is so because Q_{24} is briefly driven into saturation, and takes a while to actually turn off. As soon as Q_{21} and Q_{22} conduct, a short, non-current limited, short-circuit of the supply arises. It is for this reason that the 555 requires particular attention to be paid to decoupling of the supply voltage (see Fig. 5a). Output switching from high to low causes fewer problems because Q_{21} and Q_{22} are not driven into saturation; hence, the switch-off time is short relative to that of Q_{24} . CMOS versions of the 555 generally do suffer from this annoying effect.

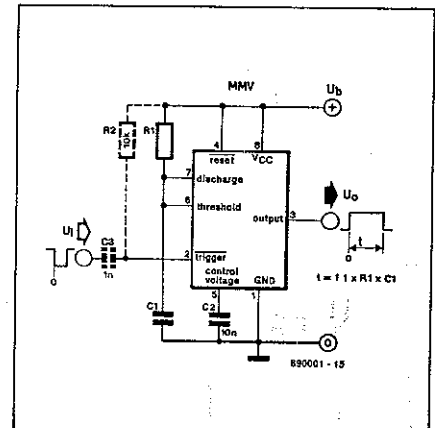


Fig. 6. Standard application of the 555 in MMV configuration.

Applications

In 9 out of 10 applications of the 555, the chip is used as a monostable or astable multivibrator (AMV or MMV respectively). In MMV configuration, the pulse time is determined by the time needed to charge the timing capacitor from 0 V to $\frac{2}{3}U_b$, the threshold voltage. In general, the charge voltage, U_c , on a capacitor, C , charging through a resistor R , from a supply voltage, U_b , is equal to $\frac{2}{3}U_b$ when

$$U_c(t) = U_b(1 - e^{-t/RC})$$

from which,

$$\tau = (-\log_e \frac{1}{3})RC \approx 1.1RC$$

The charge voltage also determines the monotime, provided the trigger pulse is shorter than the monotime. A longer trigger pulse also results in a longer output pulse, but this may be prevented by driving the trigger input with an AC-coupled signal only (add R_2/C_3 , with $(R_2C_3) < (R_1C_1)$).

The MMV circuit is turned into an AMV simply by making it self-triggering. Capacitor C_1 , via R_1 and R_2 , is charged to $\frac{2}{3}U_b$ in time interval t_1 :

$$t_1 = (-\log_e \frac{1}{3})(R_1 + R_2)C - (-\log_e \frac{2}{3})(R_1 + R_2)C = 0.694(R_1 + R_2)$$

and is then discharged again, this time only via R_2 . The discharge time, t_2 , equals

$$t_2 = 0.694R_2C$$

This means that the voltage on the capacitor toggles between $\frac{1}{3}U_b$ and $\frac{2}{3}U_b$. The total period, T , is calculated as

$$T = t_1 + t_2 = 0.694(R_1 + 2R_2)C$$

and the frequency, f_0 , as

$$f_0 = 1/T = 1.44 / (R_1 + 2R_2)C$$

It should be remembered, however, that C_1 has to be charged from 0 V when power is first applied, or when the reset input is made high. The first part of the first output period, therefore, has a period of $1.1R_1C_1$.

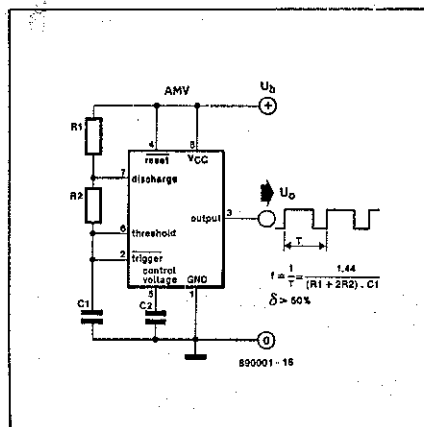


Fig. 7. Standard application of the 555 in AMV configuration.

One of the nice features of the 555 as an MMV or AMV is that the pulse time is, in principle, independent of the supply voltage, U_b . When this drops, the trigger and threshold voltages, as well as the charge- and discharge currents, drop accordingly, resulting in no change overall. A disadvantage of the AMV circuit shown in Fig. 7 is its inability to supply an output signal of duty factor greater than 0.5: this is because the charge resistance, $R_1 + R_2$, is always greater than the discharge resistance, R_2 by itself. The basic circuit in Fig. 8 shows how this can be resolved with the aid of a diode, D_1 . During charging, it bypasses R_2 , so that the charge current can become smaller than the discharge current. Another diode, D_2 , is optional if R_1 alone is to determine the charge current. It should be noted that the above use of diodes sacrifices, at least partly, the 555's independence of the supply voltage level — when the supply voltage is changed,

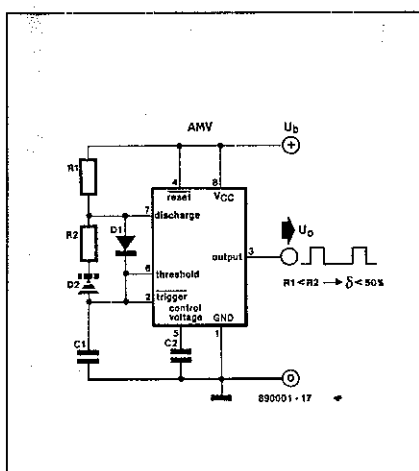


Fig. 8. Non-standard AMV configuration that allows duty factors lower than 0.5 to be achieved.

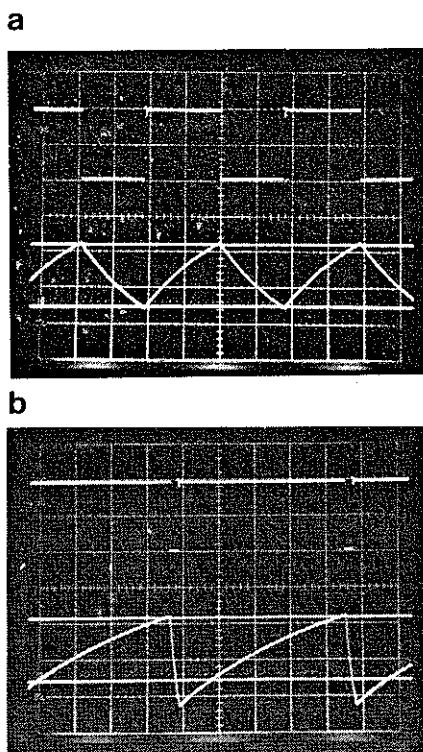


Fig. 9. Frequency deviation of a 555 in AMV configuration is a function of a number of parameters, including the duty factor. The effect shown by these oscillograms is mainly on account of the recovery time of the trigger comparator and discharge transistor. Upper trace: output signal; lower trace: voltage on timing capacitor. The horizontal traces show the trigger and comparator threshold levels.

the fixed drop across the diode results in a non-proportional change of the charge and discharge current of C_1 .

The control voltage input, pin 5, of the bipolar 555, is normally decoupled to ground with a 10 nF capacitor for noise protection. According to the manufacturers, this capacitor is no longer required with the new CMOS versions of the 555

Timing errors

It is not so simple to express the inaccuracy of a timing interval produced by a 555 as a single error-percentage. A large number of factors should be taken into account here, but many can be forestalled by correct dimensioning and/or selection of the most appropriate type of 555 for a particular application. Tolerance on the internally generated reference voltages, in combination with input-offset voltages of the trigger- and threshold comparators, introduces timing errors of the order of 2%. Internal reaction and recovery times also form a factor to be taken into account. The oscilloscope photographs in Fig 9 illustrate the behaviour of a 555-based AMV at a relatively high output frequency. Figure 9a shows the AMV set to

a duty factor of about 0.6. The frequency, 29 kHz, already deviates considerably from the calculated 25 kHz. Fig 9b shows the output signal of the same circuit, this time dimensioned for a much greater duty factor. Since the total resistance $R_1 + 2R_2$ is equal in both cases, it might be expected that the output frequency remains unchanged. It is seen, however, that C_1 is actually discharged to below the trigger level (which, like the threshold level, is marked by a horizontal trace) This effect is caused partly by the relatively quickly falling voltage on C_1 , and partly by the slowness of the trigger comparator in combination with the recovery time of the discharge transistor. Because of the excess discharge of C_1 , the output frequency of the 555 will be significantly lower than calculated: 20 kHz in this case.

The essence of all this is that the accuracy of relatively high output frequencies depends largely on the duty factor.

When the 555 is configured as an MMV, due account should be taken of the saturation voltage of the internal discharge transistor. The level of this saturation voltage is inversely related to the value of the charge resistor, and, at relatively short monetimes, causes the output pulse to be shorter than calculated.

At very low output frequencies, factors such as the leakage current of the timing capacitor, that of the discharge transistor, and the input current of the threshold comparator, become increasingly significant.

In general, the lower the frequency, the higher the values of the charge and discharge resistors. As the charge current decreases, the importance of various leakage currents increases. Also remember that the use of an electrolytic capacitor with high leakage and tolerance in position C_1 will cause a much higher timing error.

Using the control input

The control voltage input, pin 5, affords a number of interesting, yet little used,

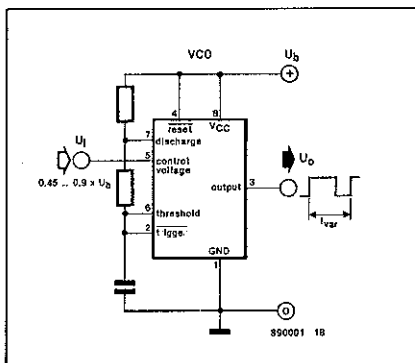


Fig. 10. By using the control voltage input, a 555-based AMV can be turned into a VCO.

app
cuss
The
con
Wh
a v
vari
sup
is m
com
whi
put
com
diag
The
trol
a vo
shov
figu
quer
In p
volt
side
min
for
achi

Fig.
mul

The
use
able
star
cho
con
volt
0 V
Wh
the
volt
of
cor
the
sist
mir
cur
high
volt
from

IRI-

In

applications, whose background is discussed below.

The internal diagram shows that pin 5 is connected to the internal voltage divider. When not externally loaded, this carries a voltage of $\frac{2}{3}U_b$. According to the manufacturers, this voltage may be varied between 45% and 90% of the supply voltage. When the control voltage is made too high, however, the threshold comparator will cease to work correctly, while a too low voltage at the control input upsets the bias point of the trigger comparator (refer to the internal diagram in Fig. 3).

The most evident application of the control voltage input is, of course, the 555 as a voltage-controlled oscillator (VCO), as shown in Fig. 10. The 555 itself is configured as an AMV whose output frequency can be varied over about $\pm 50\%$. In practice, especially when the supply voltage is relatively high, a value considerably lower than $0.45U_b$, but with a minimum of about 1.5 V, is permissible for the control voltage. The frequency so achieved becomes up to $2f_0$.

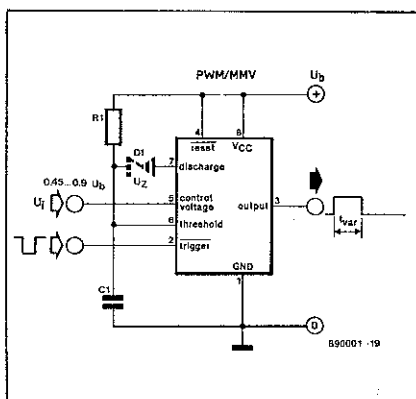


Fig. 11. Voltage-controlled monostable multivibrator.

The basic circuit of Fig. 11 shows that the control voltage input may also be used for making an MMV with adjustable monotime. When, however, the standard monostable configuration is chosen, the output pulse can never become too short. Assuming an input voltage, U_i , at pin 5 of $0.45U_b$, the voltage on C_1 will be kept at virtually 0 V by the internal discharge transistor. When a relatively large control range of the output pulse is desired, the lowest voltage on C_1 may be raised with the aid of a zener diode, or a number of series-connected, forward-biased, diodes, in the collector line of the discharge transistor. To obtain a well-defined minimum voltage on C_1 , the quiescent current through R_1 , I_{R1} , must be just high enough to achieve the correct zener voltage, U_z . This current is calculated from

$$I_{R1} = (U_b - U_z) / R_1$$

In practice, a few mA will suffice to

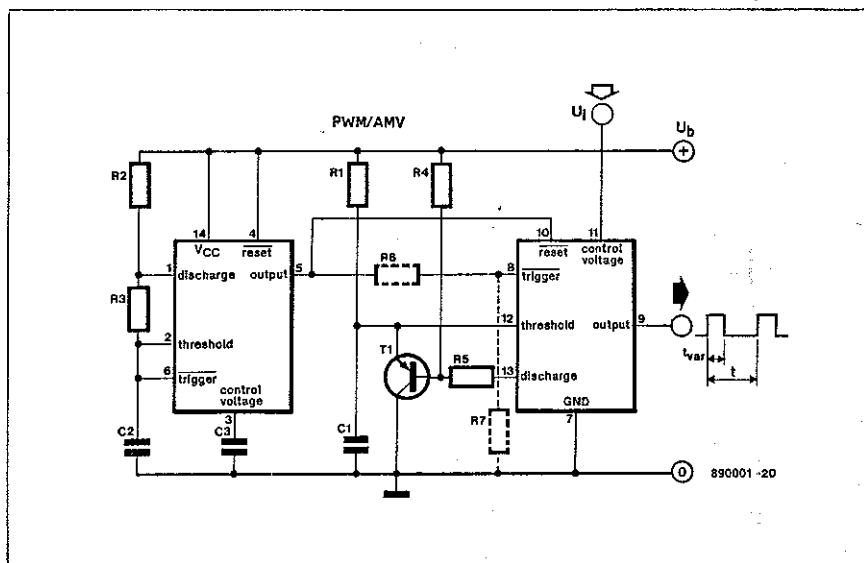


Fig. 12. Two 555's, or, in this case, a single 556, make an excellent fixed-frequency pulse-width modulator for low-loss power control systems.

achieve the zener effect

The circuit of Fig. 11 does not provide a linear relationship between control input voltage and output pulse-width. Such linearity can be achieved, however, by replacing R_1 with a current source. A practical example and a detailed explanation of this interesting configuration is given in Ref. 1.

It is fairly simple to change the basic voltage-controlled monostable into a pulse-width modulated oscillator — see Fig. 12. All that is required is another AMV-based oscillator, set up around the other 555 contained in the 556 chip. The resulting circuit is an excellent, low-loss, pulse-width modulator for use with a power-transistor driver stage.

There are a few more interesting details in the circuit shown in Fig. 12. The first has to do with C_1 , which is not discharged to 0 V, but to a level set with p.d. R_4 - R_5 , plus the base-emitter drop of T_1 . Similar to the previously discussed 'zener-trick', this arrangement considerably magnifies the span of the output pulse-width.

The second interesting point of the circuit entails the simultaneous resetting and triggering of MMV₂ to ensure an accurately defined voltage on C_1 at the start of the each period. In the absence of the trigger signal, a curious phenomenon would take place when the duty factor is, theoretically, as close as possible to 1. During the first period, the threshold voltage is not reached, so that C_1 is not discharged. Immediately after the start of the second period, however, the threshold level is reached, so that the output goes low. The result of this sequence would be the halving of the output signal frequency, and a reduction of the duty factor from almost 1 to about 0.5.

As already said, this effect is prevented by resetting the MMV at the start of

each period. Referring back to the internal diagram, the bistable is actually set and reset at the same time. Reliable triggering is, however, still ensured by virtue of the internal reset circuit switching off faster than the trigger circuit (Q_{15} has been driven into saturation, and has a longer recovery time). Incidentally, the recovery time of the trigger circuit can be shortened by using a potential divider that provides a trigger level just lower than $\frac{1}{3}U_b$.

In the concept discussed here, the duty factor can never become 1, because the output is invariably low for the duration of the reset signal of the MMV. This is why R_3 is generally made small relative to R_2 .

The control voltage input of a standard 555 forms a fairly low resistance ($5 \text{ k}\Omega // 10 \text{ k}\Omega = 3.3 \text{ k}\Omega$ typ.). CMOS versions of the 555 have a much higher input resistance thanks to an internal voltage divider composed of three 100 k Ω resistors. In general, tolerance of these input resistance values is relatively high, so that a voltage source driving the control input should be designed to have a low output impedance.

Long-interval timers

As already hinted at in the section on timing errors, configuring the 555 as a long-interval timer may pose problems because of the inevitable role of leakage currents in the timing components, i.e., the high-value resistor(s) and the capacitor. A further aggravating effect is that the leakage current of an electrolytic capacitor is age- and temperature-dependent. In practice, the maximum interval that can be achieved with a 555 in standard configuration is 10 to 30 minutes long, taking a fairly high tolerance for granted.

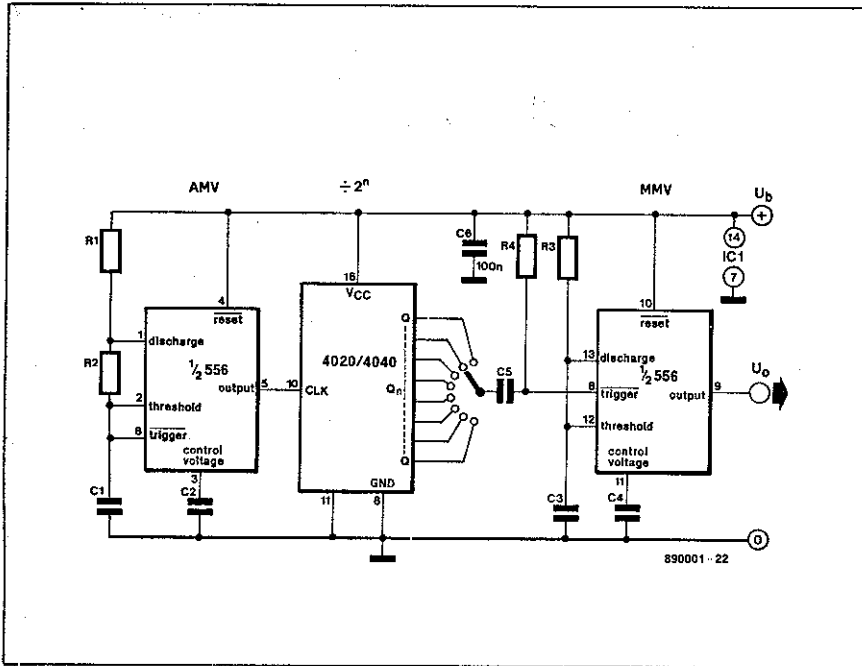


Fig. 13. Long-interval timers are best realized with the aid of a ripple-cascade divider.

One solution to obtain better-defined and longer intervals would be the cascading of 555s, so that each is triggered by the previous one. This is not a very neat solution to the problem, however, since all timing errors of individual timers in the cascade simply add up (accumulation effect). Moreover, the duration of the interval rises only linearly with the number of 555 stages. The increase can be made exponential by following one 555 in AMV mode with a divider as shown in Fig. 13. Depending on the application, the *n*-th output of the divider can trigger a further 555, this time in MMV mode. In this set-up, the 555 in AMV mode is conveniently dimensioned for optimum accuracy (average values for *R*₂ and *R*₃, and a low-leakage capacitor for *C*₁), while cascaded dividers afford timer intervals of hours, days or even weeks.

CMOS versions: 7555 and TLC555

Intersil was the first to introduce the 7555, a CMOS version of the 555. A little later, Texas Instruments, in line with its consistent and successful policy of producing LinCMOS (linear CMOS) versions of 'bipolar bestsellers', came up with the TLC555. As with a number of well-established opamps and comparators, the TLC555 and TLC556 from TI were an instant success.

In general, current consumption of the CMOS versions has been drastically reduced with respect to the bipolar 555 — from 10 mA to 100 μA, while the minimum supply voltage has been lowered to 2 V. Obviously, these features are of great importance for the design of

battery-powered circuits. The CMOS versions do not suffer the large peak current at output switch-over, while the input bias current of the threshold comparator, and the leakage current of the discharge transistor, are also significantly reduced. These features of the new devices are advantageous because they allow a higher charge resistance for the capacitor, bringing longer timing intervals within reach.

Thanks to the virtual absence of saturation effects commonly associated with bipolar transistors, speed of the new CMOS 555's has also increased. In a laboratory test, a standard 555 gave up

at about 180 kHz, whereas a 7555 scored 1.1 MHz, and a TLC555 even 2.4 MHz (test conditions: AMV configuration with *R*₁=*R*₂=220 Ω and *C*₁=100 pF). As far as output current is concerned, however, the bipolar 555, with its sink and source capability of 200 mA, is still superior to the CMOS versions. The 7555 supplies a maximum of 5 to 50 mA, depending on the supply voltage (10 mA at 10 V). The TLC555 has a symmetrical output with a source and sink capability of 10 mA and 100 mA respectively. Ergo, where the replacement of a standard 555 with a CMOS type is considered, the current requirement of the load should be taken into account (a standard 555 is often used to power a relay direct).

Reference:

- 1 Long-range infra-red transmitter-receiver. *Elektor Electronics* November 1987; p 40 and 41

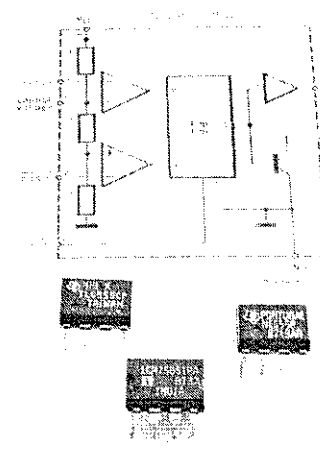


Table 1

	555			7555			TLC555			unit
	min.	typ.	max	min.	typ.	max	min.	typ.	max	
V _{cc} /V _{dd}	4.5		18	2		18	2		18	V
Supply current	2V									0.25
	5V	3	5	0.08	0.4		0.17	0.35		mA
	10V	10	12	0.12	0.6		0.36	0.60		mA
Output Current	I _{sink}	200		8	80		100			mA
	I _{source}	200		1	20		10			mA
Threshold current		100	250		10		0.01			nA
Discharge state-off current		20	100		10		0.1			nA
MMV timing error		1	3		2		1	3		%
Temp. drift			500		250					ppm/°
V _{cc} drift			0.5		0.3	1		0.1	0.5	%/V
Output	rise-time	100	300	75			20			ns
	fall-time	100	300	75			75			ns
f _{max}			0.5		1		2			MHz

data valid at T_a = 25 °C

Ind
rote
sim
oth
spe
duc
con
mo
con
of t
trol
ter
spe
dire
requ
circ
disc
squi

A
The
mot
sim
form
at e
(see
this
a tir
of tl
shor
ly
disn
The
with
this
One
the s
plyit
maint
90°