THE MULTI-MAC CONCEPT

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ITT's Digit-2000 system has been designed to ensure ready integration of new TV and audio standards with existing hardware concepts. This means that a MAC decoder based on the Digit-2000 system is readily installed into an existing TV set as an upgrade. Provided the necessary control software is available, it is, of course, also possible to use the relevant chip set in a stand-alone application, which is of particular interest to the many thousands of viewers who own satellite-TV receiving equipment. This article introduces the main components that go into the making of such a C/D/D2-MAC compatible decoder.

Intermetall/ITT Semiconductors is among the world's largest producers of components for the consumer electronics market. Since 1985, the company has been involved in the development of MAC decoding systems, and it was the first semiconductor manufacturer to introduce a D2-MAC decoder chip, the DMA2270. The planned use of D-MAC on the BSB services, among other factors, prompted ITT Semiconductors to expand the DMA2270 with a multi-MAC decoding feature. The result is the C-, D- and D2-MAC compatible DMA2280, which, together with the DMA2285 MAC descrambler, forms the heart of the multi-MAC decoder for the Digit-2000 system.

An important point must be made at this stage. When we speak of a MAC decoder, we mean a circuit capable of extracting video and audio information from a signal to the MAC standard. As such, the function of the MAC decoder may be compared to that of, say, an FM decoder. Hence, the use of the word 'decoder' has in principle nothing to do with scrambling, and is really a misnomer. Just like PAL TV signals, or, for that matter, FM radio signals, MAC signals may be encrypted. Since that process has basically nothing to do with the standard of the transmission—only with the way in which the input signal is pre-processed—a separate unit, the MAC descrambler, may be used along with the MAC decoder. As already stated, the associated type numbers in this context are DMA2285 and DMA2280 respectively. The use of the DMA2285 is optional. However, bearing in mind that all BSB channels are encrypted, a MAC descrambling chip like the DMA2285 is a must for all BSB receive units.

Digit-2000: ready for the future

The Digit-2000 concept is illustrated in Fig. 1. Signals travel from the left (signal sources) to the right (sound/picture re-

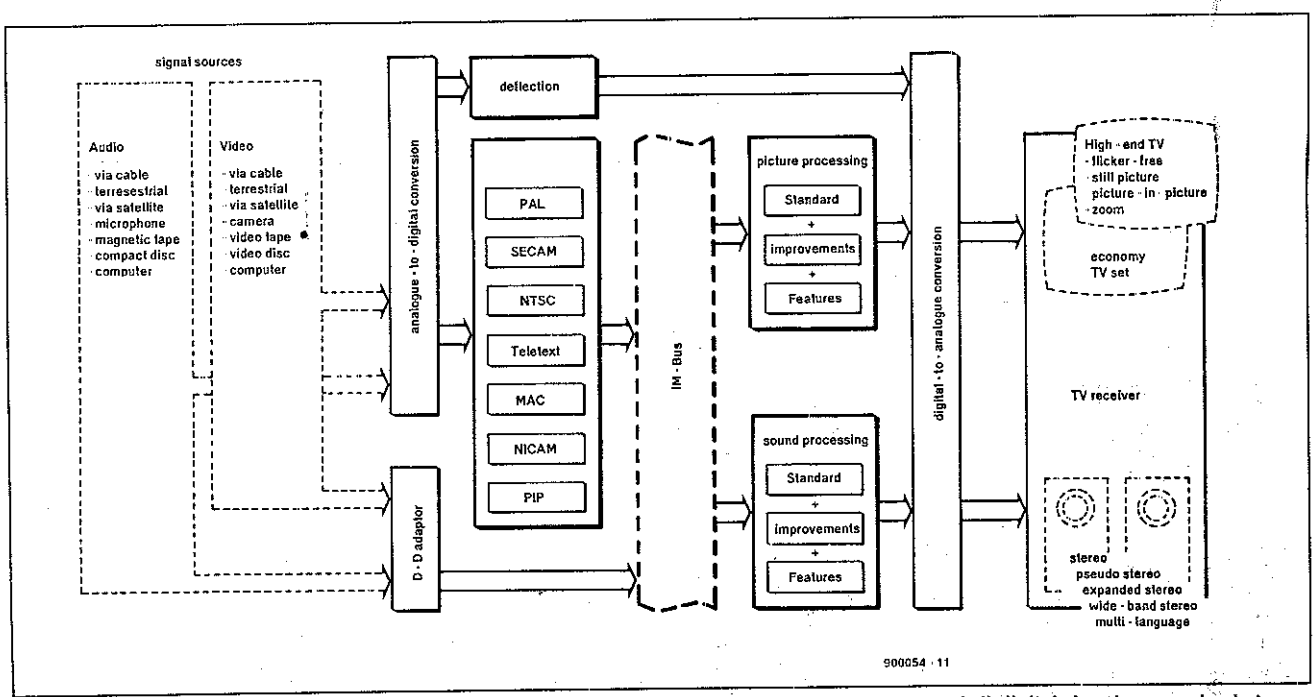

Fig. 1. ITT's Digit-2000 TV/radio system is geared to easy expansion by virtue of a command bus and all-digital signal processing between an ADC and a DAC.

production devices) The intermediate signal processing is entirely digital between an ADC and a DAC Control signals for the system are conveyed via the IM bus, which is a simple 4-wire network that enables a central or external processor to communicate with the various devices (slaves) connected to the bus The system is very flexible in that it allows new standards to be implemented readily Take, for instance, the MAC extension: it is driven by the same ADC, is controlled by the same bus, and uses the same DAC as, say, the PAL circuitry This means that the system allows both an economy and a top-quality TV set to be produced on the basis of three main building blocks: a fast ADC, a control bus, and a fast DAC Extensions are always possible in this system: the appropriate unit (say, a NICAM processor) is simply connected in parallel with existing circuits and addressed via the IM bus

MAC in a nutshell

The PAL, NTSC and SECAM colour TV systems currently in use are based on frequency division, which means that the two video components and the sound component are assigned a particular part of the transmitted spectrum In this system, it is virtually impossible to ensure perfect separation of the luminance ('brightness') and chrominance ('colour') information Inevitably, signals of both components will encroach upon each other's part of the frequency spectrum — see Fig 2a The effect is the well-known moiré patterning in picture areas with relatively fast luminance transitions The colour processor in the TV receiver mistakes these fast luminance signals in the cross-colour area between about 2 3 MHz and 3 5 MHz (PAL) for colour information, and actuates colours which are not related to the luminance information in the particular picture area

MAC relies on time division rather than frequency division and gives near-perfect separation of the picture components Figures 2b and 2c shows how the luminance (Y) picture components in a PAL video signal may be transferred and compressed at a ratio of 3:2 into a time slot in the MAC signal (Ref 1) The chrominance component (compression ratio: 3:1) is transferred in a similar manner to the time slot preceding the Y period MAC lines alternately carry the compressed U (B–Y) and V (R–Y) colour difference signals Note that both Y and U/V are analogue levels Compression and expansion are required to fit these signals into the available line time, which is 64 µs just as with PAL.

Each line of MAC consists of serial U/V and Y signals, reference periods and a sound/data burst (packet) The latter is digital and duobinary-encoded (Ref 2) to reduce the bandwidth of the FM signal produced for D- and D2-MAC transmissions via satellite D-MAC differs from D2-MAC by its higher data rate in the sound/data burst: 20.25 MHz instead of 12 125 MHz (Fig 2d), which allows a greater number of high-quality sound channels to be used at the expense of a slightly greater bandwidth.

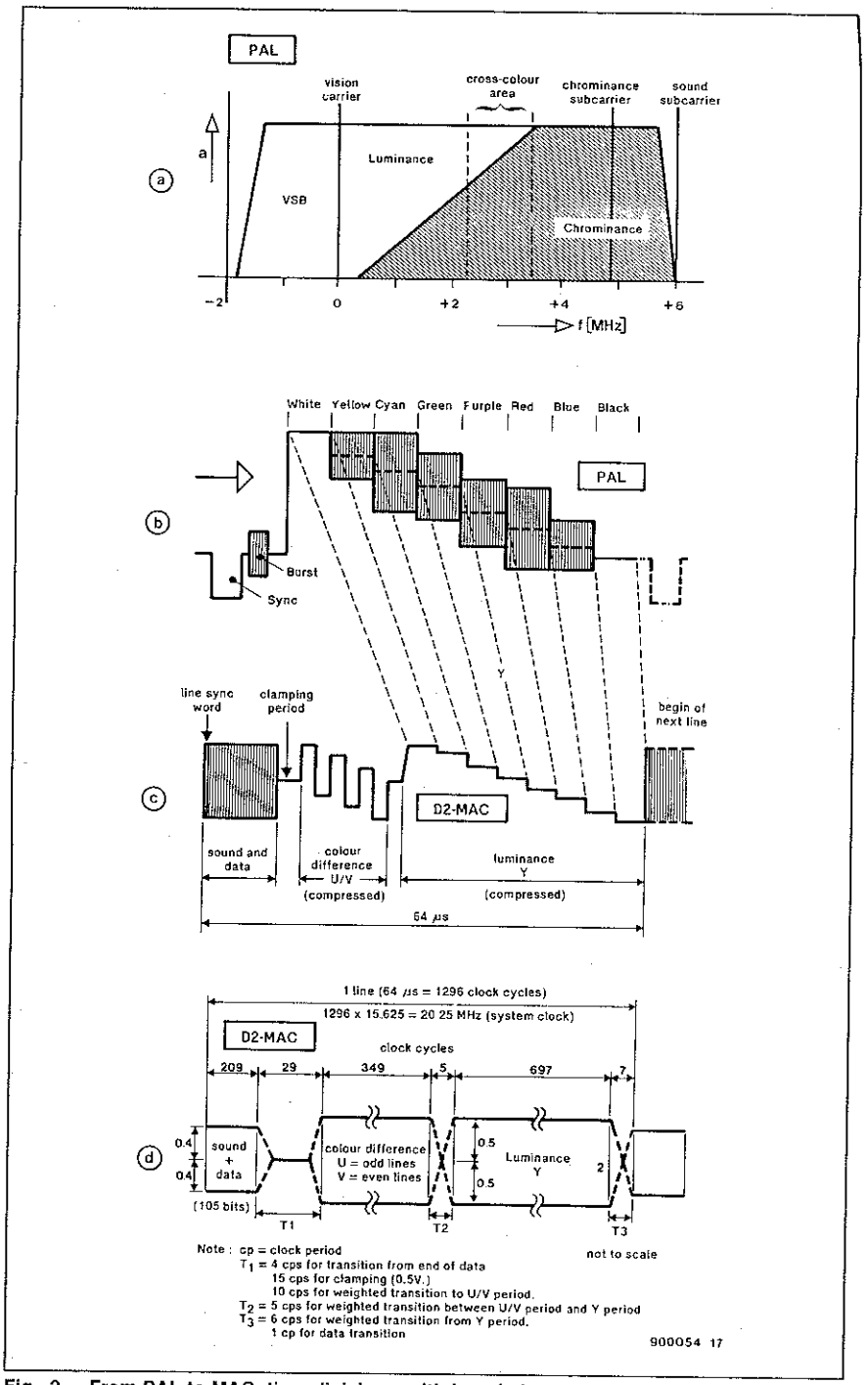

Fig. 2. From PAL to MAC: time-division multiplex of picture components and sound.

Clock generator MCU2600

After a necessarily brief recap on the background of MAC, the components that go into ITT's Multi-MAC concept will be discussed below with reference to block diagrams. Unfortunately, the scope of this article does not allow a full description of each device to be given; this may be found in the relevant datasheets

Time multiplexing must rely on accurate clocking of various circuits in the MAC decoder As shown in Fig 2d, the system clock required for a MAC signal is determined by the number of samples within the line time of 64 µs, and the line frequency: 1,296/15,625 = 20 25 MHz

The MCU2600 supplies the digital processors, decoders converters, etc, that form part of the Digit-2000 TV system with the required main clock signal, which is of trapezoidal shape, with rounded corners, to avoid cross-talk and other interference The MCU2600 may also be used for PAL SECAM or NTSC: depending on the crystal used, the chip

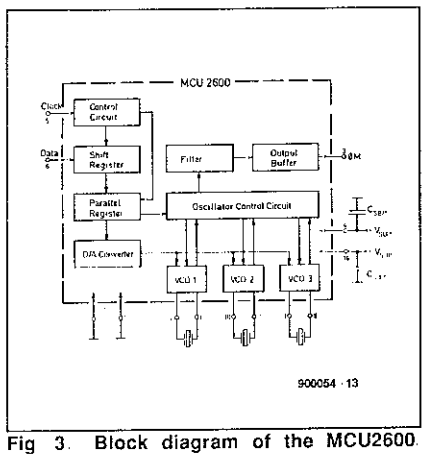

Fig 3. Block diagram of the MCU2600.

supplies four times the chroma subcarrier frequency needed (PAL/SECAM: 17 734 MHz; NTSC: 14 318 MHz).

All three VCOs on board the MCU2600 may be selected individually, via the clock and data inputs, to form part of a PLL which is controlled by another chip, for instance, the DMA2280 MAC decoder. The PLL control (= error-) signal is applied in digital serial form to pin 6 of the MCU2600. The default VCO selection is VCO1.

Video coder/decoder (codec) VCU2133

The VCU2133 contains the ADC and the DAC mentioned above in the introduction of the Digit-2000 concept. The chip is provided with the baseband signal after de-emphasis to the MAC standard (which is not the same as the CCIR standard for PAL). As already noted, all digital signal processors in the Digit-2000 system are located between the ADC and the DAC in the VCU2133, which provides the following functions (see Fig 4):

- two software-selectable input amplifiers
- one fast A-D converter for the composite video signal
- one noise inverter
- one D-A converter for the luminance signal
- two D-A converters for the colour difference signals
- one RGB matrix for converting the colour difference signals and the luminance signals into RGB signals
- three RGB output amplifiers
- programmable auxiliary circuits for blanking, brightness adjustment, white balance control and picture tube alignment
- additional clamped RGB inputs for text, teletext or other analogue RGB signals
- programmable beam current clamping

The VCU2133 may be used with a variety of video circuits, including the VPU2203 PAL processor, the CVPU2233 NTSC Comb Filter Video Processor, the SPU2220 SECAM Chroma Processor, the DPU2553 Deflection Processor and the DTI2223 Digital Transient Improvement Processor (note: DTI is sometimes referred as CTI: colour transient improvement). The chip contains a large number of registers that are loaded and read by the central processor in the Digit-2000 system via the IM bus.

The A-D converter that follows the two video input amplifiers and the selection switch is of the flash type, which means that it is a circuit that consists of 2^n comparators in parallel. For a slowly varying video signal, 8 bits are required. To achieve 8-bit picture resolution with a 7-bit converter, a special operation known as 'bit enlargement' is used. During every other line, the reference voltage of the A-D converter is changed by an amount corresponding to one half of the least-significant bit (LSB). In this manner, a grey value between two 7-bit steps is converted into the next lower value during one line, and into the next higher value during the next line. The two grey values are averaged by the viewer's eye, producing the impression of grey values with 8-bit resolution. Synchronously with the changing reference voltage of the ADC, a half-bit step is added to the output signal of the Y DAC every second line. The bit enlargement is switched off for D- and D2-MAC signals by appropriate control of the registers in the VCU2133.

The ADC's sampling frequency supplied by the MCU2600 is 17.7 MHz (PAL/SECAM), 14.3 MHz (NTSC) or 20.25 MHz (MAC). The converter's resolution is ½ LSB of 8 bits. Its output signal is Gray-coded to eliminate spikes and glitches resulting from different comparator speeds, or from imperfections in the coder itself.

After having been processed in other circuits, e.g., the DMA2280, the different parts of the digitized video signal are fed back to the VCU2133 for further processing to drive the RGB output amplifiers. The luminance (Y-) signal is routed from the contrast multiplier in the DMA2280 to the Y DAC in the VCU2133 in the form of a parallel 8-bit signal with a resolution of ½ LSB of 9 bits. This range provides enough headroom for large contrast vari-

ABBREVIATIONS

ADC	Analogue-to-Digital Converter
AGC	Automatic Gain Control
ALU	Arithmetic Logic Unit
BER	Bit-Error Rate
BSB	British Satellite Broadcasting
CCIR	Comité Consultatif International de Radio
CCU	Central Control Unit
CLIMB	Command Language for Intermetall Bus
DAC	Digital-to-Analogue Converter
FM	Frequency Modulation
HD-MAC	High-Definition MAC
MAC	Multiplexed Analogue Components
NICAM	Near-Instantaneous Companding Analogue Multiplex
NTSC	National Television Standards Committee
PAL	Phase Alternation Line
PC	Personal Computer
PDM	Pulse Duration Modulation
PLL	Phase-Locked Loop
QPSK	Quadrature Phase Shift Keying
RGB	Red-Green-Blue
ROM	Read-Only Memory
SECAM	Séquentiel Couleur à Mémoire
SEEPROM	Serial Electrically Erasable Programmable Read-Only Memory
VCO	Voltage-Controlled Oscillator

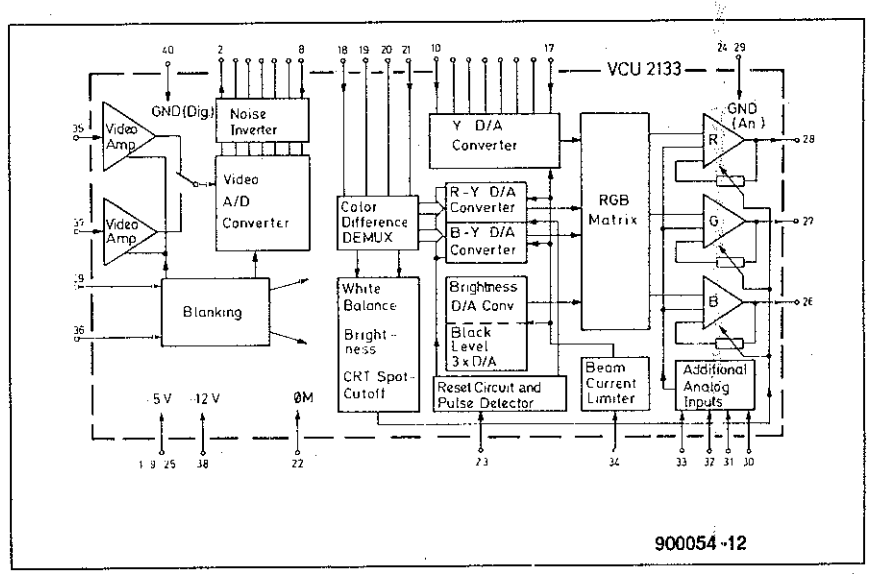

Fig 4 Block diagram of the VCU2133 ADC/DAC.

ations as well as positive and negative overshoot The Y DAC is an R-2R ladder network which is provided with the central clock frequency (20 25 MHz for MAC)

The two digital colour difference signals, R–Y and B–Y, are transferred in a time-multiplex arrangement to save on input pins At a clock of 20 25 MHz and a chrominance bandwidth of between 1 MHz and 2 MHz, this can be done with impunity Like the Y DAC, the two 8-bit DACs for R–Y and B–Y are implemented as R-2R ladder networks Although they are clocked at one quarter of the central clock frequency, the multiplex data transfer rate is 20 25 MHz (for MAC) Sixteen (four times four) bits are transferred sequentially under the control of a sync signal that co-ordinates the multiplex operations between the VCU2133 and the video processor (in this case, a DMA2280)

C/D/D2-MAC decoder DMA2280

This chip forms the heart of the multist ard MAC decoder Its tasks may be summarized as follows:

- to accept the digitized video (baseband) signal and extract from this the time-compressed chrominance and luminance information, and the sound/data packet
- to de-compress (expand) and correlate the luminance and chrominance information
- to extract audio, special data and sync words from the sound/data packet, taking account of the two different data rates (D2-MAC: 10 125 MHz; D-MAC: 20 25 MHz)
- to ensure a central clock of 20 25 MHz by providing a control voltage to the PLL in the MCU2600
- recognition of packet 0 for special purposes
- when required to provide error correction on weak input signals, and allow different slicing levels to be defined for the on-board duobinary decoder
- provide an AGC signal for (digital) level control of the baseband input signal
- to communicate with the central IM bus processor

The DMA2280 is the multi-MAC version of the (older) DMA2270. Its block diagram is given in Fig. 5 The DMA2280 is a complex chip by almost any standard because it handles many relatively fast digital signals at the same time It has on-board luminance and chrominance storage circuits which enable the relevant picture components to be de-compressed (expanded) and multiplexed (chrominance only) under the control of the central clock Furthermore, it is capable of de-interleaving and linking the packets sent in each MAC TV line. A special word recognizer with error correction capabilities ensures the recognition of the field and line syncs, which are complex digital words contained in the sound/data packet The DMA2280 has a capability for direct interfacing with any of the teletext processors in the Digit-2000 series, such as the TPU2733

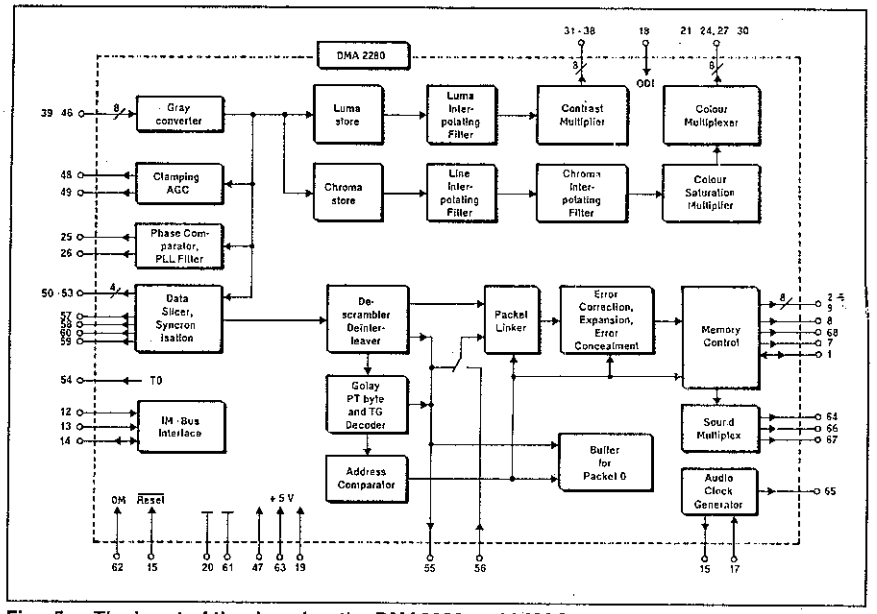

Fig. 5. The heart of the decoder: the DMA2280 multi-MAC processor.

The sound recovered from the data packets is fully decoded by the DMA2280 but left digital for demultiplexing and converting into analogue form by the AMU2485 audio processor

All functions provided by the DMA2280 are controlled by registers, of which the content is determined by the chip itself (read-only) or the central processor The bit-error rate (BER) register, for instance, contains a number that represents the sum of the error bits encountered in the 82 packet headers in one frame This sum is stored in a register that can be read as bits 0–7 at address 206 by the central processor, which can take the necessary actions such as muting the audio signal when the BER parameter exceeds a certain predefined level The DMA2280 occupies a total of 12 addresses on the IM bus The bits reserved for these registers control a total of over 30 programmable functions, some of which may be used to select, in turn, up to four different modes of operation. The selection between C-, D- and D2-MAC is not automatic and must therefore be accomplished by the control software.

It should be noted that the DMA2280 requires a separate sound demodulator for C-MAC, since in that case the sound is provided in 2-4 QPSK rather than duobinary FM

Audio mixer AMU2485

The AMU2485 (Fig 6) receives the serial audio data supplied by the DMA2280 at its S-bus inputs The S-bus is unidirectional and consists of three lines: S-clock, S-ident and S-data The sound information is transmitted in frames of 64 bits, divided into four successive 16-bit sam-

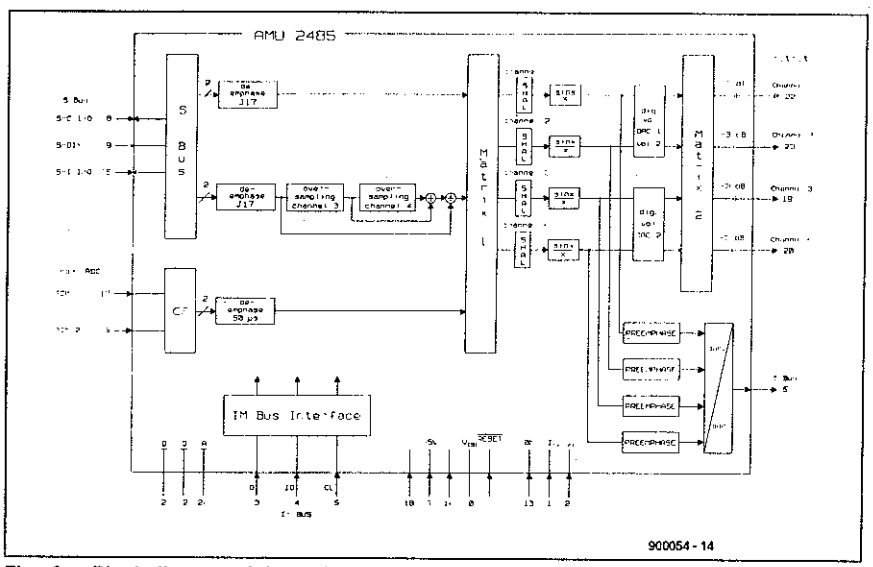

Fig. 6. Block diagram of the audio component in the decoder, the AMU2485.

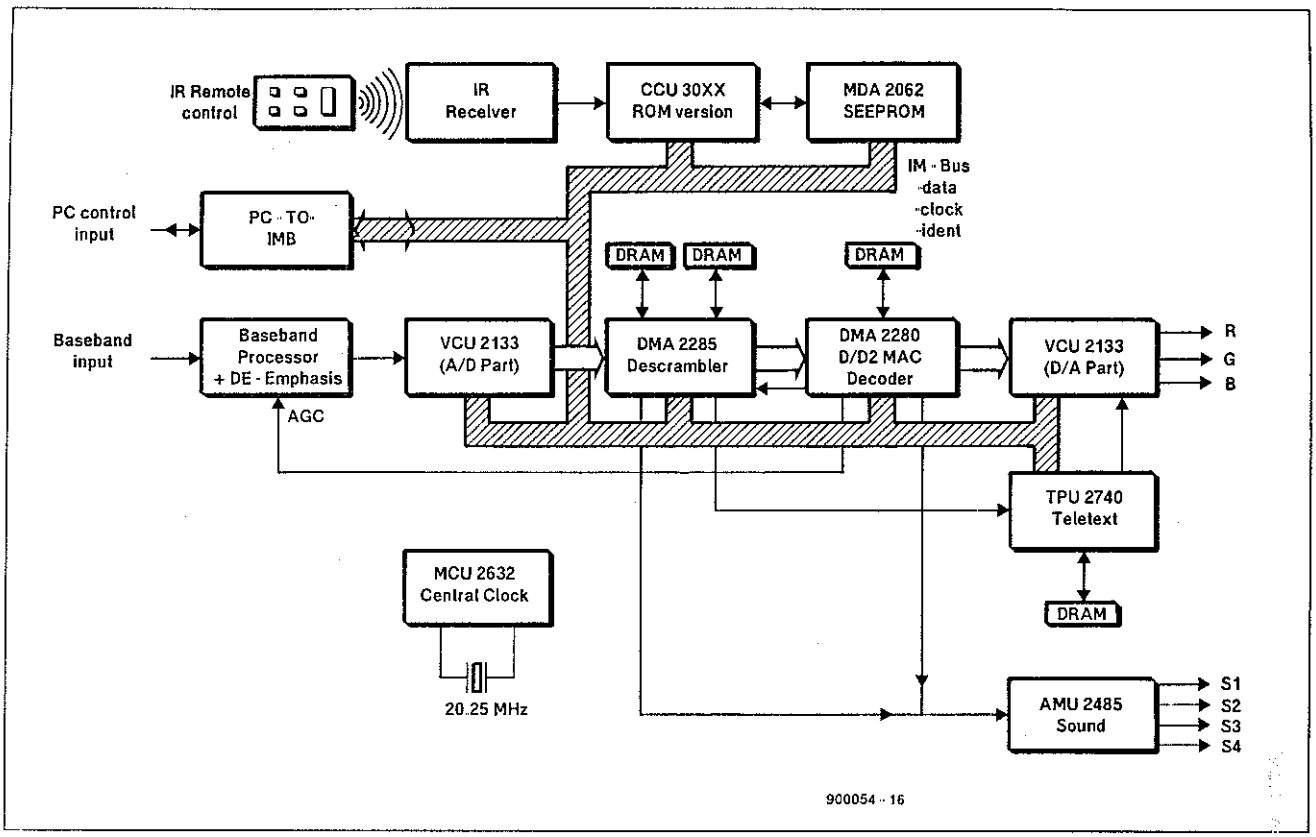

Fig 7. Block diagram of a multi-standard MAC decoder intended for use as a set-top box The PC-to-IMB interface is required during the development stages only

ples Each sample represents one audio channel The repetition rate of the samples is equal to the sampling rate of the D- or D2-MAC signal so that up to four sound channels can be transferred simultaneously

The AMU2485 provides a complete digital signal processor that runs its own control program from an on-chip mask-programmable ROM Two de-emphasis filters are available: one to the CCIR J17 standard (used for MAC and NICAM transmissions) and one to the 50 µs standard (used for PDM sound broadcasts) Both de-emphasis circuits operate digitally and can be switched off if required by an appropriate register instruction

The oversampling filters in S-bus channels 3 and 4 allow medium-quality D2-MAC sound signals (16 kHz sampling rate) to be mixed with high-quality signals (32 kHz sampling rate) The filters are third-order Cauer-type low-passes with a stop-band rejection of 40 dB

The audio mixing feature of the AMU2485 allows any input to be routed to any output and, of course, to mix differently weighted input channels The mixing and volume control operations on the DACs are entirely digital and run under the control of an internal ALU that receives the appropriate commands via the IM bus

A multi-MAC decoder

The previously discussed chips all go into the making of the MAC decoder shown in Fig 7 This concept packs all the signal processing required between the baseband output of the indoor unit and the RGB drivers in the colour monitor or TV set into a single set-top decoder

The IM bus, which has not been discussed so far, is shown as a shaded path that links the sub-circuits into a small network The bus consists of three lines: Signal Ident (ID), Clock (CL) and Data (D) The clock frequency range is 50 Hz to 170 kHz Ident and clock are unidirectional from the CCU to the slave devices; data is bidirectional to allow the CCU to interrogate devices by loading and examining the contents of their registers

The block diagram in Fig 7 shows that the decoder can be controlled either by a PC via the PC-to-IMB interface, or by a CCU which uses a SEEPROM for storing and loading user settings such as the MAC standard (C, D, or D2), sound selection or contrast The PC is required only during the development stages of the decoder; the software that runs on it, CLIMB, allows all registers in the chips that form the decoder to be examined and, if necessary, loaded or reloaded CLIMB allows individual chips such as the VCU2133 to be programmed in great detail, with the aim of developing machine code for the CCU

Once debugged and tested, the system control software is burned into a ROM on board the CCU The CCU, which may be a 65xx or 80xx-like processor, has a direct input for digital data supplied by an infrared receiver

As shown in the block diagram, the DMA2280 works in conjunction with the DMA2285 descrambler In addition to its normal function as a low/high level MAC decryption processor, the DMA2285 allows 16:9 format HDMAC pictures to be converted to 4:3 format Note, however, that this feature makes the decoder described only partly compatible of HD-MAC because of the present resolution of 625 lines Fortunately, the next generation of MAC chips —which are now being developed — will be capable of meeting the full HD-MAC specification with 1,250 lines and thus deliver virtually flicker-free wide-format pictures ■

Source:
Datasheets AMU2485; DMA2280; DMA2285; VCU2133; MCU2600/2632; DMA2270; CLIMB V2 1 **ITT Semiconductors**.

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References:
1. The MAC system *Elektor Electronics* July/August 1987
2 Introduction to duobinary encoding/decoding *Elektor Electronics* January 1990

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 10REM>FILTEMUL/2
 20MODE20
 30 INPUT"Sweep over how many octaves (0 = CW) "oct%
 40 INPUT"Signal-to-noise ratio in dB "K
 50 INPUT"Pink-factor for noise (1=white noise; >1=pink noise) "P%
 60K=1/(10^(K/20))
 70 INPUT"Co-efficient a for Y(T)=a.x(T)+(1-a)Y(T-1) "A
 80IF A<0 OR A>1 THEN 70
 90 INPUT "Order of filter "ord%
100PROCsweep
110PROCnoise
120PROCnoisy_signal
130PROCfilter
140GCOL0,1:MOVE0,800:FORT%=0TO1279STEP3:PLOT5,T%,S(T%)+800:NEXT
150REM -- NOISE ---MOVE0,400:FORT%=0 TO 1279:PLOT5,T%,N(T%)+400:NEXT
160GCOL0,2:MOVE0,500:FORT%=0TO1279:PLOT5,T%,SN(T%)+500:NEXT
170GCOL0,3:MOVE0,200:FORT%=0TO1279:PLOT5,T%,F(T%)+200:NEXT
180END
190:
200DEFPROCsweep
210 REM --- SINE-WAVE DATA ---
220DIM S(1280)
230W=.003*PI
240FORT%=0TO 1280
250S(T%)=100*SIN(W*T%*(1280+oct%*T%)/1280)
260NEXT
270ENDPROC
280:
290DEFPROCnoise
300REM --- NOISE DATA ---
310DIM N(1280)
320FOR T%=0 TO 1280
330N(T%)=K*(RND(100)-RND(100))
331IF P%<2 THEN 390
340noise=N(T%)
350FOR n%=0 TO P%
360N(T%)=noise
361IF T%=1280 ENDPROC
370T%+=1
380NEXT n%
390NEXT T%
400ENDPROC
410:
420DEFPROCnoisy_signal
430DIM SN(1280)
440SN()=S()+N()
450ENDPROC
460:
470DEFPROCfilter
480DIM F(1281)
490FOR T%=1 TO 1279
500F(T%)=A*SN(T%)+(1-A)*F(T%-1)
510NEXT
520 FOR ord%=1 TO ord%
530FOR T%=1 TO 1279
540F(T%)=A*F(T%)+(1-A)*F(T%-1)
550NEXT
560NEXT
570ENDPROC
580:
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Fig. 8. Acorn Archimedes program that demonstrates some basic procedures in signal recovery from noise.

modern CD player is an example of this. Analogue signals corrupted by noise can also be 'cleaned' by the RISC computer. The listing of Fig. 8 is a demonstration program written in BBC BASIC V. It should be borne in mind that the program is only intended to become acquainted with the basics of software-based filtering of noisy signals. The program as shown may be modified for running on other computers than the Archimedes, but calculation times will be unacceptable in many cases. The program prompts the user to enter the desired signal-to-noise ratio and the order of the filter, and demonstrates the possibility of recovering, in theory, a signal even when this has an S/N ratio of 0.

The hardware approach to noise filtering may be demonstrated with the basic ciruit shown in Fig. 8. The filter is usable for signals between 100 and 2500 Hz, and can be clocked by an external source (5 to 60 kHz).

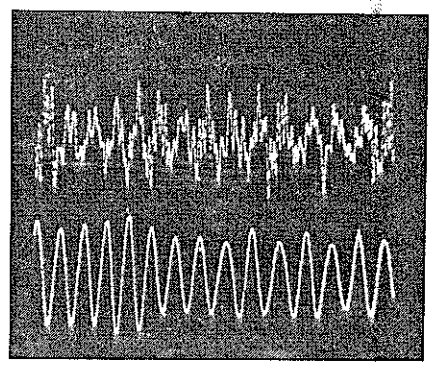

Fig. 10. The results of the circuit of Fig. 9 are remarkable given the simplicity of the design.

There is very little doubt that RISC-based computer systems running dedicated error-correction software will eventually become so fast as to enable run-time, digital, enhancement of video signals. This has been partially achieved already with a combination of hardware and software MAC TV decoders, of which the first types are expected to become available commercially later this year.

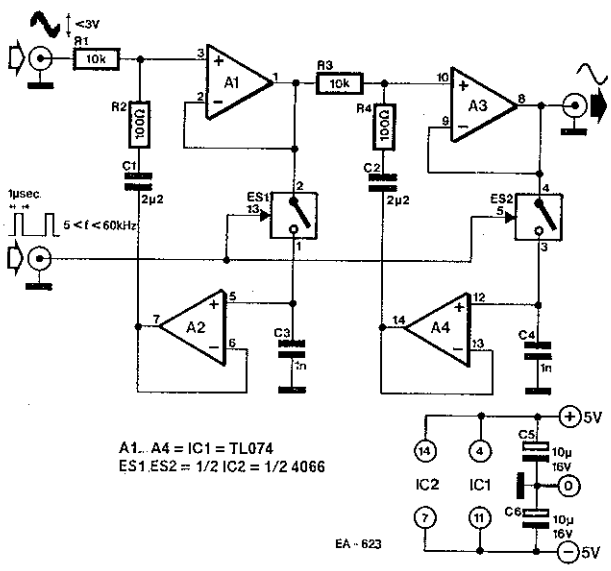

Fig. 9. Experimental noise-suppression circuit.