Adjustment of the primary section is effected by setting P1 to obtain a reading of 1 mA through a milliammeter connected in place of JP1.

The signal received by the photo-transistor in the opto-isolator is amplified by a second LF356 whose gain is controlled by P2. After the LED current has been set, this preset may be adjusted to ensure unity gain of the entire amplifier.

The circuit needs two completely separate power supplies and this means two transformers or one transformer with two isolated secondary windings. The primary section needs a symmetrical supply, whereas a single 8–15 V supply will suffice for the secondary section. ■

(J. Ruffell)

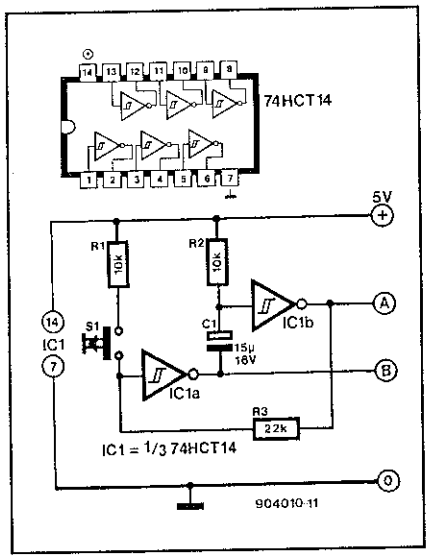
DEBOUNCING CIRCUIT WITH TWO OUTPUTS

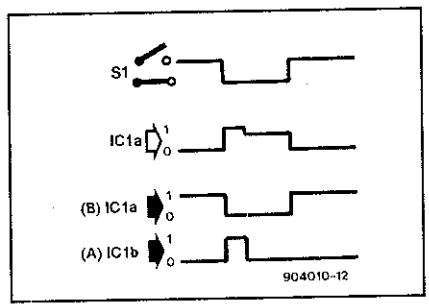
005

Any switch or key in a digital circuit may cause problems because mechanical contacts bounce up and down a few times before they close. Normally, this weakness is negated by an RS bistable, but this article shows that it also may be achieved by a monostable.

The two gates in the circuit diagram form a monostable with a mono time of 100 ms (the bounce time of a key is typically 20 ms).

In quiescent operation, the input of inverter IC1b is at the level of the supply voltage, so that its output is low. This low level is connected to the input of IC1a via R3. The output of IC1a is thus high and C1 is not being charged.





When the switch, S1, is closed, the input of IC1a goes high because R1 has a smaller value than R3. The output of IC1a then becomes zero, which is immediately connected to the input of IC1b via C1. This low level remains at the input during a time determined by R2-C2. Any bounce of the switch during this time has no effect whatsoever, because the output of IC1b, and thus the input of IC1a, is high.

When a switch or key is released, it will be noticeable at output B but not at output A, because C1 needs time to discharge. Only after it has discharged, can the monostable be triggered again.

The gates should be CMOS types, preferably of the HC/HCT series. The circuit works best with Schmitt trigger inverters, although most run-of-the-mill inverters work perfectly well.

The current drawn from the supply is negligible. ■

(From an idea by H. Smits)

CLOCKWISE AND ANTI-CLOCKWISE DC MOTOR CONTROL

006

This straightforward circuit, based on four darlingtons, enables a d c motor to rotate clockwise or anti-clockwise under the control of two digital signals provided by, say, a computer.

As may be seen from the diagram, the circuit consists of two identical sections. Concentrating on the left-hand section, when a high logic level (+5 V) is applied to input I1, T2 is switched on and a current can flow to earth via D1. I1 is cut off, because its base is negative with respect to its emitter owing to the voltage drop across the diode (–0.6 V). When a low logic level (0 V) is applied to I1, T2 is cut off and I1 obtains base current via R1. The motor can then draw current via I1.

The right-hand section operates in an identical manner.

By applying different logic levels to the inputs, that is, logic high to I1 and logic low to I2, or vice versa, the motor may be made to rotate clockwise or anti-clockwise, as the case may be. When the levels at the inputs are identical, the motor is at a standstill.

With component values as shown, motors needing up to 45 V at 2 A may be controlled. However, when the current exceeds 0.5 A, the transistors need heat sinks.

The circuit may be used to control the motor speed by pulse-width modulation. This requires a constant level at one input (depending on the direction of rotation), while the pulses are applied to the other input. ■

(R. Mennis)