MOUNTING STRIPLINE-OPPOSED-EMITTER (SOE) TRANSISTORS

INTRODUCTION

The Stripline Opposed Emitter (SOE) package presently used by Motorola for a number of rf power transistors represents a major advancement in high frequency and thermal performance. This Application Note discusses the SOE package, it advantages and limitations as well as a number of considerations to avoid improper usage

An understanding of a few basic principles in regard to mounting and heat-sinking of this package can help avoid cases of poor performance or device damage.

Two general package types – the stud-mounted and flange-mounted SOE packages will be discussed. Each of the general types is available in a variety of sizes. Typical package outlines of the two SOE packages are shown in Figure 1.

ADVANTAGES OF THE SOE PACKAGE

The primary electrical advantages of the SOE packages are the low inductance strip line leads which interface very well with the microstrip lines often used in UHF-VHF equipment and the good collector to base isolation provided by the two emitter leads. The two emitter concept promotes symmetry in board layout when combining devices to obtain higher output power. Both emitter leads should always be used for best performance.

DESCRIPTION OF THE SOE PACKAGE

Figure 2 displays the component parts on a stud-mounted SOE package. This package will be used as an example since both the stud and flange-mounted packages are very similar in construction. The body of the package is a Berylium Oxide (BeO) disc. Berylium Oxide was chosen due to its high thermal conductivity. Attached to the bottom of the disc is a copper stud which is for heat transfer and mechanical mounting. The lead frame is attached to a metalized pattern on to the top surface of the BeO disc. The actual shape of the leads differs between the various package types. Finally an Alumina ceramic cap is attached to the top of the disc over the leads providing a protective cover for the transistor die.

An understanding of the basic structure of the SOE package is essential to proper usage of these devices in respect to heat-sinking and mechanical mounting. Since these two areas present the greatest problem to users, they will be discussed in detail.

HEAT-SINKING THE SOE PACKAGE

In order to properly understand the thermal considerations involved in mounting SOE type packages, it is necessary to lay some groundwork in the area of heat flow. Table I gives equivalent Thermal and Electrical parameters which may be used to relate Thermal properties to more familiar electrical units.

Semiconductor power devices are usually guaranteed to have a certain thermal performance as stated by the thermal resistance of the device from the junction to the case, or mounting surface – θ_{JC}. How to get the heat out of the

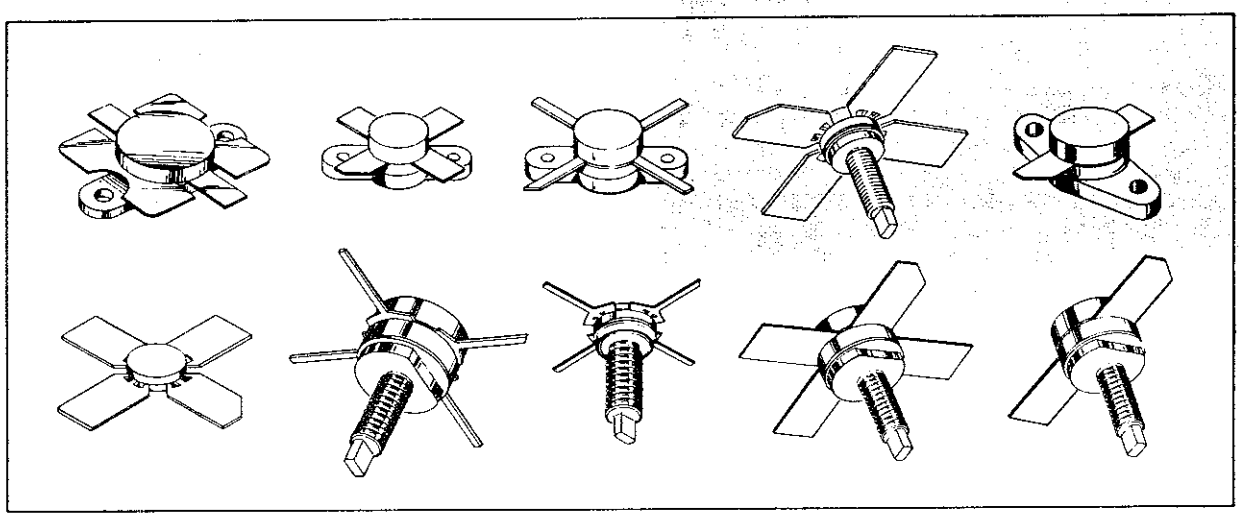

FIGURE 1 – SOE Packages

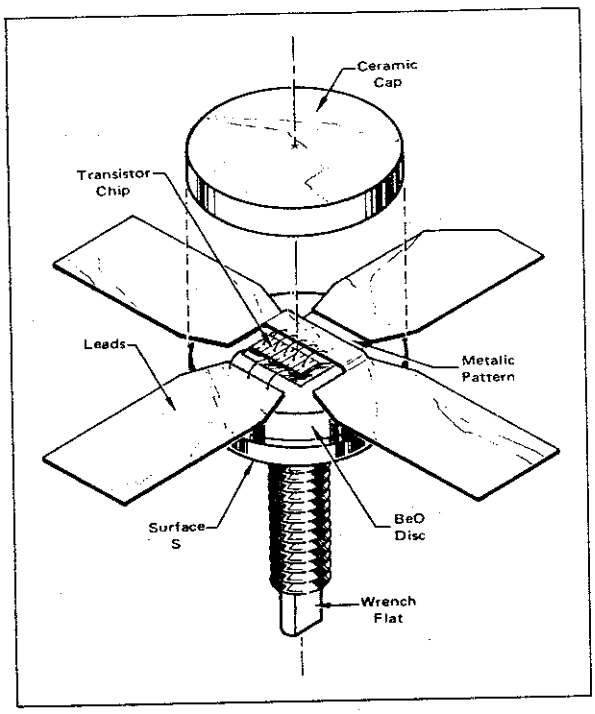

FIGURE 2 – Component Parts of SOE Package

case has generally been left to the user. In any dynamic heat flow problem, the heat must go somewhere, otherwise there will be a continuous rise in the temperature of the system. In text books, there always seems to be an "infinite heat sink" available which can absorb any amount of heat with no temperature rise whatsoever. In the practical sense, however, such a heat sink does not really exist. Practical heat sinks must be characterized by a certain temperature rise for a given ambient condition, with a known amount of heat input (power to be dissipated) after equilibrium conditions have been achieved. Characterization of heat-sink systems is best achieved by examining the complete system under controlled conditions.

TABLE I – Thermal Parameters and Their Electrical Analogs

Symbol	Thermal Parameter	Units*	Electrical Analog	
			Symbol	Parameter
ΔT	Temperature difference	^{o}C	V	Voltage
H	Heat flow	watts	I	Current
θ	Thermal resistance	^{o}C/watt	R	Resistance
γ	Heat capacity	$\frac{\text{watt-sec}}{^{o}C}$	C	Capacity
K	Thermal conductivity	$\frac{\text{cal}}{\text{sec-cm-}^{o}C}$	σ	Conductivity
Q	Quantity of heat	cal	q	Charge
t	Time	sec	t	Time
$\theta\gamma$	Thermal time constant	sec	RC	Time constant

*Note the one major difference in thermal and electrical units: Q is in units of energy, whereas q is simply a charge. Hence H is in units of power and may be equated to an electrical power dissipation.

For example, the normal environment for a land-mobile VHF transmitter might be the trunk of a taxi cab in the hot Arizona summer. In such an environment, temperatures might reach as high as 80°C (176°F). The heat-sink system for such a radio should therefore be tested at a minimum ambient temperature of 80°C. The method that should be applied in this test would utilize a fine wire thermocouple rigidly secured to the stud of the rf power transistor for which the test is being conducted. The system, which in this case would include all parts of the radio which would contribute heat, should then be operated under maximum heat generating conditions in the high temperature environment specified. Careful measurement of the temperature of the device under test would then give the difference in temperature between the case of the transistor and the controlled ambient.

If the case and ambient temperatures are known, as well as the power levels in the transistor, the thermal resistance from the transistor case to the ambient can be calculated. The first step is to obtain the power being dissipated by the device

$$P_d = P_1 + P_2 - P_3 \qquad (1)$$

where: P_d = power being dissipated by the transistor in watts;

P_1 = dc power into the transistor in watts;

P_2 = rf power into the transistor in watts;

P_3 = rf power out of the transistor in watts.

This value of P_d is used to obtain the θ_{CA} value from the equation:

$$\theta_{CA} = \frac{T_C - T_A}{P_d} \qquad (2)$$

where: θ_{CA} = thermal resistance device case to ambient;

T_C = device case temperature;

T_A = ambient temperature.

In order to determine the maximum temperature rise in the transistor element (junction temperature rise) under any given operating condition the following equation may be used.

$$T_j = (\theta_{JC} + \theta_{CA})P_d + T_A \qquad (3)$$

where: T_j = junction temperature;

θ_{JC} = published thermal resistance – junction to case.

If power is dissipated in a power transistor, the case temperature will rise above the ambient temperature by an amount determined by θ_{JC} and θ_{CA}. Since the value to θ_{JC} is fixed by the transistor type being used, θ_{CA} is the only factor with which the user can control the junction temperature for a given power dissipation.

Since heat generated by the transistor must be radiated to the ambient by the heat sink, a low θ_{CA} requires an effective heat sink. In general, an efficient heat sink requires that material with high thermal conductivity and high specific heat be used. A table of thermal properties for various materials is given in the Appendix. A well-designed heat sink requires that all thermal paths be as short as possible and of maximum cross-sectional area. Examples of thermal resistance calculations for a bar and a flat disc of thermal conducting material are given in the Appendix.

The equations given in the Appendix however, assume no thermal resistance between the case and the heat sink.

The primary heat conducting surface on stud-mounted SOE packages is the flat metal surface between the actual stud and BeO case body labeled surface S in Figure 2. This surface, which has a D-flat on some case types, must make good contact with the heat sink to allow good thermal conduction. To insure good contact: a) the heat sink mounting surface must be flat, b) the mounting hole must be burr free, the proper size and perpendicular to the mounting surface, c) the proper sized nut should be used and d) the nut should be properly torqued. Recommended mounting hardware is given in the section on device mounting.

With flange-mounted devices the primary parameters affecting thermal transfer are the flatness of the heat sink surface and the flatness of the device flange. The flange-mounted package requires that good contact be made between the flange and the heat-sink surface, particularly directly beneath the BeO disc.

With either of these packages it has been found that a considerable improvement in thermal transfer can be achieved through the proper use of one of the silicone based "heat-sink compounds" which are marketed by several vendors. Dow Corning and Wakefield Engineering are both suppliers of good thermal compounds. It should be pointed out however, that these compounds have a thermal conductivity approximately equal to that of Mica (0.0018 Cal/Sec-cm-^{o}C) which is poor compared to that of Aluminum (0.49 Cal/Sec-cm-^{o}C). However by comaprison, the thermal conductivity of still air is approximately 0.000006 Cal/Sec-cm-^{o}C). The quantity of silicone grease used must be kept to the absolute minimum required to fill in any air gaps which might occur between the transistor mounting surface and the heat-sink surface. In the case of the stud-mounted package this is the gap after the transistor has been secured with the proper stud torque. Contributions of as high as 0.5^{o}C/watt to the overall thermal resistance can occur if the heat-sink compound is used in a sloppy and excessive manner.

MOUNTING SOE DEVICES

The second area demanding consideration by a user of SOE transistors is mechanical mounting. Failure to observe proper mounting procedures can result in device destruction. This section will discuss both the stud-mounted, and the flange-mounted SOE devices.

Seven general considerations for properly mounting SOE transistors are listed briefly below. More detailed discussion will follow.

A. The device should never be mounted in such a manner as to place ceramic to metal joints in tension.

B. The device should never be mounted in such a manner as to apply force on the strip leads in a vertical direction towards the cap.

C. When the device is mounted in a printed circuit board with the copper (stud or flange) and BeO portion of the header passing through a hole in the circuit board, adequate clearance must be provided for the BeO to prevent shear forces from being applied to the leads.

D. Some clearance must be allowed between the leads and the circuit board when the device is properly secured to the heat sink.

E. The device should be properly secured into the heat sinks before the device leads are attached (soldered) into the circuit.

F. The leads must not be used to prevent device rotation on stud type devices during stud torque application. A wrench flat is provided for this purpose.

G. With stud packages, maximum stud torque, as stated later in this note, and on the respective device data sheets must not be exceeded. If repeated assembly/disassembly operation is expected, a lesser torque should be used.

Most of the considerations listed above are designed to prevent tension at the metal-ceramic interfaces on the SOE package. Improper mechanical design can lead to application of stresses to these joints resulting in device destruction. Three joints are considered: The cap to the BeO disc, the leads to the disc, and the stud or flange to the disc.

The joint between the ceramic cap and the BeO ceramic disc is composed of a material which loses strength above 175^{o}C. While the strength of the material returns upon cooling, any force applied to the cap at high temperature may result in failure of the cap to ceramic joint.

The lead frame and stud or flange attachment will be grouped together since they are very similar. Although the SOE package used by Motorola makes use of high temperature ($> 700^{o}$C) solder alloys for lead frame and flange or stud attachment, care should be taken to avoid the application of tensile forces to the joint in the mounting of the transistor into a system. Such forces could result if the device were mounted with improper mounting clearances.

MOUNTING THE STUD TYPE SOE TRANSISTOR

Figure 3 shows a cross-section of a printed circuit board and heat sink assembly for mounting a stud type SOE device. Let us define H as the distance from the top surface of the printed circuit board to the D-flat heat sink surface. If H is less than the minimum distance from the bottom of the lead material to the mounting surface of the SOE

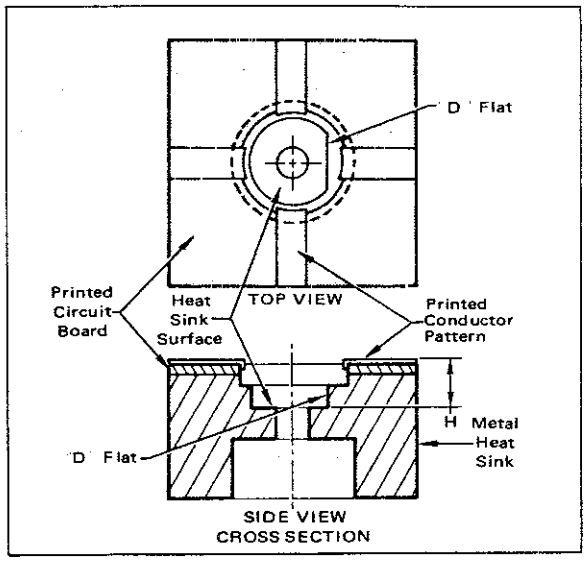

FIGURE 3 – Typical Stud-Mounting Method

package, there is no possibility of tensile forces in the copper stud – BeO ceramic joint. If, however, H is greater than the package dimension, considerable force is applied to the cap to BeO joint and the BeO to stud joint. Two occurances are possible at this point. The first is a cap joint failure when the structure is heated, as might occur during the lead soldering operation; while the second is BeO to stud failure if the force generated is high enough. Lack of contact between the device and the heat sink surface will occur as the difference between H and the package dimension becomes larger, this may result in device failure as power is applied.

Proper stud torque is an important consideration when mounting stud type SOE devices.* The stud section of the SOE package is composed of a special copper alloy chosen because of its high thermal conductivity. However when this material is used in studded semiconductor device packages, it is necessary to place severe restrictions on the amount of tightening torque which can be applied to a nut used to secure the device to a heat sink.

*The Motorola Outline Dictionary calls for Class 2A threads. The National Bureau of Standards Handbook H28 entitled Screw Thread Standards, paragraph 4.2 on page 2.17, reads in part as follows:

> 'However, for threads with additive finish, the maximum diameters of Class 2A threads may be exceeded by the amount of the allowance; i.e., the 2A maximum diameters apply to an unplated part or to a part before plating whereas the basic diameters (the 2A maximum diameter plus allowance) apply to a part after plating."

Also, footnote b, page 2.37 reads:

> For Class 2A threads having an additive finish, the maximum is increased to the basic size the value being the same as for Class 3A."

This means that for plated parts, the no-go gauge used is the 2A minimum and the go gauge used is the 2A maximum plus the allowance or in other words the 3A maximum.

The recommended torque values are listed below for the two thread sizes presently being employed on Motorola rf power transistor packages.

Recommended maximum torque for stud SOE transistors follows:

	8 - 32 Threads	10 - 32 Threads
One time maximum	6.5 lb.-in.	11.0 lb.-in.
Repeated assembly-assembly maximum	5.0 lb.-in.	8.5 lb.-in.

An evaluation of the effects of measured torque on the studs under consideration requires a known set of conditions. The system used to generate the data shown in Figure 4 consisted of a 1/8 inch aluminum plate with a deburred clearance hole for the stud under test, a steel washer to be positioned between the plate and appropriate steel nut. A calibrated torque wrench was used as the driving means. On each unit under test, the spacing separating four threads positioned between the nut and heat-sink surface was measured. After mounting the device on the aluminum plate and applying a known amount of torque the spacing was again measured and the results recorded.

The results of this test show that up to the maximum torque specified, the permanent elongation of the threads increases linearly with applied torque. At the torque specified this elongation does not exceed acceptable limits.

MOUNTING THE FLANGE TYPE SOE TRANSISTOR

The mounting and heat sinking of the flange type package is similar to that of the stud type package. The main considerations with the flange package are avoiding tensile stresses at the metal-ceramic joints and providing a flat heat conducting surface beneath the flange.

Figure 5 shows a typical mounting technique for flange type SOE rf power transistors. Again H is defined as the distance from the top of the printed circuit board to the heat-sink surface. If distance H is less than the minimum distance from the bottom of transistor lead to the bottom surface of the flange, tensile forces at the various joints in the package are avoided. However, if distance H exceeds the package dimension, problems similar to those discussed for the stud type devices can occur. Because of the ability

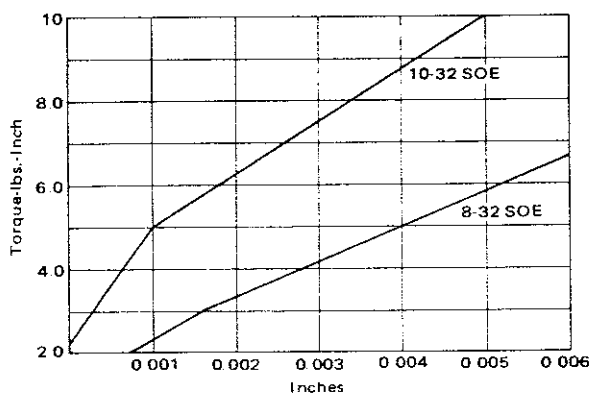

FIGURE 4 – Permanent Elongation Over a Four Tooth Length

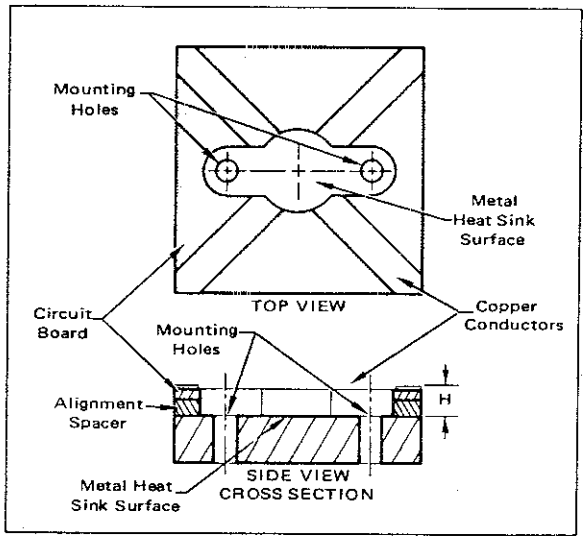

FIGURE 5 – Flange Type SOE Transistor Mounting Method

of the copper flange to bend under the types of loads encountered when the mounting screws are tightened, permanent deformation of the flange may result. Corrective action after the flange has been bent will not necessarily insure proper thermal contact with the heat sink.

The flange surface as supplied with Motorola SOE transistors is either flat or slightly convex. It is important that the mating heat-sink surface also be flat or slightly convex to provide the best contact when the device is properly secured.

The holes for the mounting screws should be deburred because any irregularity of the surface at these two points is equivalent to concavity of the heat-sink surface which will degrade thermal contact between the transistor and the heat sink.

Since the flange may be permanently deformed during mounting, the device should not be dismounted and remounted in another position.

CONCLUSION

The SOE package is an excellent rf power transistor package. However, improper heat sinking and mechanical mounting can result in device damage. A number of considerations have been presented to inform the potential user of the hazards of improper mounting. Proper usage of the SOE package requires no great difficulty if the designer is aware of the limitations and construction of the package.

A list of recommended mounting hardware and a suggested mounting procedure follows:

Table of Recommended Mounting Hardware Which Can be Supplied With Motorola Stud Type SOE Transistor

Stud Thread Size	Motorola Part Numbers		
	Nut	Flat Washer	Lock Washer
10-32	02BSB51568F044	04BSB51567F040	04BSB51566F028
8-32	02BSB51568F042	04BSB51567F038	04BSB51566F030
6-32	02BSB51568F040	04BSB51567F036	04BSB51566F032

STEPS IN A PROPER MOUNTING PROCEDURE

1. Compare the distance between the heat sink surface and the top of the printed circuit board with the minimum dimension of the transistor from the mounting surface to the bottom of the leads. The transistor dimension, as stated on the device data sheet, should be the greater distance to avoid the chance of stresses on the various joints of the SOE package.

2. Bore the proper sized mounting hole or holes for the stud or mounting screws. These holes should be perpendicular to the heat sink surface and they should be properly deburred.

3. Place a limited amount of thermal compound on the heat sink surface where it will contact the flange or mounting surface above the stud. Insert the transistor and mount with the proper hardware as suggested in the preceeding table.

   In the case of the stud device, torque the nut to the proper value.

4. Solder the leads to the printed circuit board using the minimum amount of heat and the least possible time of application. The leads should be soldered as close to the package as possible to minimize series lead inductance.

5. With the unit exposed to the highest expected ambient temperature, and power applied, measure the temperature at the stud or flange surface with a thermocouple to insure that this temperature is not excessive. Before production quantities are commited, it is suggested that a sample assembly to be tested under worst case heat generating conditions.

APPENDIX

In order to aid in heat-sink design, a table of thermal properties of common materials and a pair of thermal conductivity examples are presented.

Table AI gives three important thermal properties of common heat-sink materials. In order to evaluate materials for use in heat sinks these three thermal properties should be considered.

Thermal conductivity is a measure of the ability of a material of known cross-sectional area to transfer heat a given distance in a given time with a given temperature difference. Generally metals are good thermal conductors.

Specific heat is a measure of the amount of heat a given mass of material can accept for a given rise in temperature. The scale is normalized to the heat capacity of water ($H_2O = 1.0$).

Mass density is simply the mass per unit volume of a material. This parameter is important in heat sink design to the extent that large heat sinks of dense material carry with them a serious weight penalty.

TABLE A1 – Typical Thermal Properties of Materials

Material	Thermal Conductivity K (cal/sec-cm-°C)	Specific Heat S (cal/gm-°C)	Mass Density ρ (gm/cm°C)
Silver	0.97	0.056	10.5
Copper	0.92	0.093	8.9
Gold	0.69	0.030	19.3
Beryllia-Ceramic	0.55	0.31	2.8
Aluminum	0.49	0.22	2.7
Brass	0.26	0.094	8.6
Silicon	0.20	0.18	2.4
Germanium	0.14	0.074	5.5
Steel	0.12	0.12	7.8
Solder	0.09	0.04	8.7
Kovar	0.046	0.11	8.2
Alumina-Ceramic	0.04	0.21	3.7
Plastic-Epoxy	0.0026	0.2	2.0
Glass	0.0026	0.20	2.2
Mica	0.0018	0.20	3.2
Teflon	0.00056	0.25	2.2
Air	0.000057	0.24	0.0013
Heat Sink Compound	0.0018	–	–

Example 1

In order to present some of the important characteristics to be used in heat sink design, the examination of two admittedly simplified models is desirable. The analogy between electrical resistivity and thermal resistivity will be employed

The first of these is shown in Figure A1

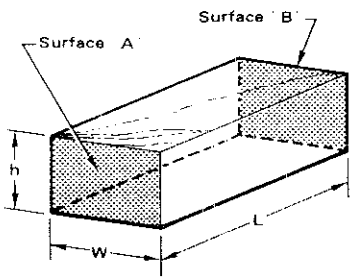

FIGURE A1 – A Bar of Thermal Conducting Material

The electrical resistance from Surface A to Surface B of this bar of conductive material is:

$$R = \frac{\rho L}{hW} \qquad (A1)$$

Using the electrical to thermal analogs:

$$\theta = \frac{L}{KhW} = \frac{1}{KA} \qquad (A2)$$

This simplified model might represent a pedestal mount or a device mount in the center of a bar connecting at either end to a housing and demonstrates the need for thermally conducting paths of high cross-sectional area and the shortest possible length

Example 2

The second simple model represents the mounting of the power device on a plate of conducting material which provides the conducting path to the ambient conditions.

Consider the simple disc geometry shown in Figure A2 as a donut-shaped sheet resistor Equation A3 represents the electrical resistance between r1 and r2,

$$R = \frac{\rho}{2\pi x} \ell n\left(n \frac{r2}{r1}\right) \qquad (A3)$$

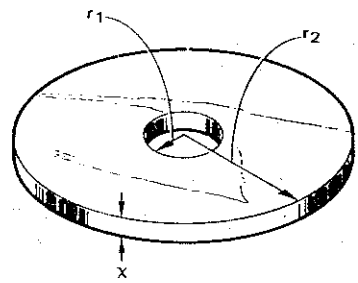

FIGURE A2 – Disc-Shaped Thermal Conductor

using the first term of the appropriate power series expansion

$$R \approx \frac{\rho}{\pi x}\left(\frac{r2 - r1}{r2 + r1}\right) \qquad (A4)$$

Where: ρ = Resistivity;

$$\rho = \frac{1}{\sigma};$$

σ = Conductivity.

Replacing the electrical terms with their thermal analogs we find:

$$\theta = \frac{1}{K\pi x}\left(\frac{r2 - r1}{r2 + r1}\right)$$

Note the inverse linear dependence of thermal resistance on the thickness of the conducting sheet.

This model demonstrates a major factor in designing heat sink structures for stud type power transistors All other factors being equal the thickness of the thermally conducting plate is of prime importance in the solution of heat flow problems