SYSTEMIZING RF POWER AMPLIFIER DESIGN

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INTRODUCTION

Two of the most popular RF small signal design techniques are:

1) the use of two port parameters, and
2) the use of some type of equivalent circuit for the transistor.

Early attempts to adapt these techniques to power amplifier design led to poor results and frustration.

In the mid-1960's, Motorola pioneered the concept of solid state power amplifier design through the use of large signal transistor input and output impedances. This system has since achieved almost universal acceptance by solid state communications equipment manufacturers. It provides a systematic design procedure to replace what used to be a trial and error process. This note is a description of the concept and its use in transmitter design.

LIMITATIONS OF SMALL-SIGNAL PARAMETERS

As a vivid example to show the short-comings of trying to adapt small-signal parameters to power amplifier design, the 2N3948 transistor was considered. A performance comparison was made of the 2N3948 operating at 300 MHz as a Class A small-signal amplifier, and as a Class C* power amplifier delivering a power output of 1 W. Table I shows the results of this comparison.

	CLASS A Small-signal amplifier V_{CE} = 15 Vdc; I_C = 80 mA; 300 MHz	CLASS C Power amplifier V_{CE} = 13.6 Vdc; P_o = 1 W
Input resistance	9 Ohms	38 Ohms
Input capacitance or inductance	0.012 μH	21 pF
Transistor output resistance	199 Ohms	92 Ohms
Output capacitance	4.6 pF	5.0 pF
G_{PE}	12.4 dB	8.2 dB

Table I — Small- and large-signal performance data for the 2N3948 show the inadequacy of using small-signal characterization data for large-signal amplifier design. Resistances and reactances shown are parallel components. That is, the large-signal input impedance is 38 ohms in parallel with 21 pF, etc.

The most striking difference in this comparison is in the device input impedance. As operation is changed from small-signal to large-signal conditions, the complex input impedance of the 2N3948 undergoes a considerable change in magnitude and actually changes from inductive to capacitive reactance.

Note also that the transistor's output resistances and power gains are considerably different for the two modes of operation. This example clearly demonstrates the inaccuracies that would result in a power-amplifier design based on the small-signal parameters of this device.

IMPORTANCE OF LARGE-SIGNAL PARAMETERS

The network theory for power amplifier design is well known but is useless unless the designer has valid input and output impedance data for the transistor. The design method described in this report hinges primarily on the direct measurement of these parameters for use in network synthesis equations. Large-signal impedance data, together with power output and gain data, provide the designer with the information necessary to design his amplifier networks and to predict the performance that should be achieved when the design is completed.

A clear understanding of the test conditions and method of presentation for the large signal impedance data is important.

TEST CONDITIONS

The term "large-signal input impedance" and "large-signal output impedance" refer to the actual transistor terminal impedances when operating in a matched amplifier at the desired RF power output level and dc supply voltage.

"Matched" is defined as the condition where the input and output networks of the test amplifier provide a conjugate match to the transistor, such that the input and output impedances of the amplifier are 50 + j 0 ohms.

Large-signal impedances should not be confused with small-signal, two port parameters which are normally measured at low signal levels with Class A bias and the transistor (or IC) connected directly to a short, open, or 50 ohm termination.

Most of the data which appears on Motorola RF power transistor data sheets is measured in common emitter, Class C amplifiers; as this condition covers the majority of device applications.

One significant exception to this involves transistors characterized for Class B linear power amplifier service. Examples of such transistors are the Motorola 2N5941-2 series. Since these transistors are designed specifically for linear service, their large-signal impedances were measured in a linear power amplifier test circuit with a two tone test signal instead of the conventional single frequency signal. For further information on these transistors see the

*Class C as used here, refers to operation with both the emitter and base at dc ground potential and with the collector supply as the only dc voltage applied, regardless of resulting device conduction angle. Usually, the emitter is connected directly to chassis ground and the base is dc grounded through an inductive network element or choke.

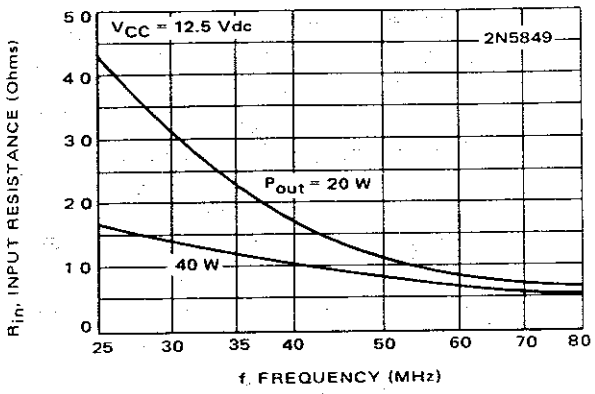


FIGURE 1 – Parallel Equivalent Input Resistance versus Frequency

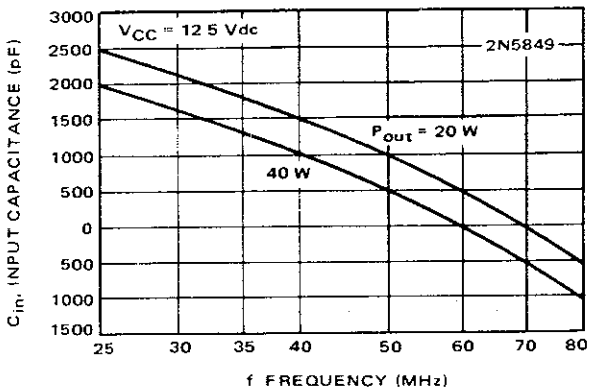


FIGURE 2 – Parallel Equivalent Input Capacitance versus Frequency

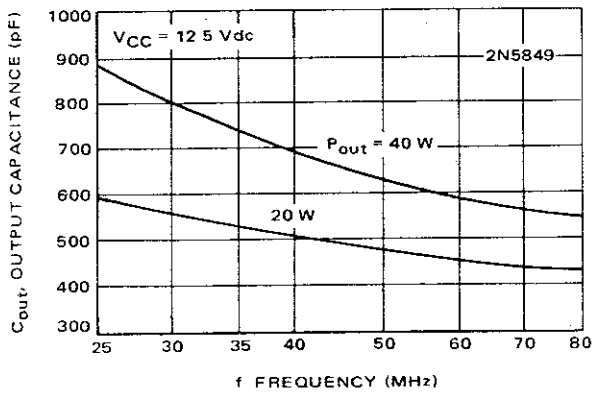


FIGURE 3 – Parallel Equivalent Output Capacitance versus Frequency

Motorola 2N5941-2 data sheet.

DATA FORMAT

Much of the information on device data sheets is presented in parallel equivalent form of resistance and capacitance. Figures 1-3 form an example of this type of presentation. The data may also be presented in series equivalent form. It makes no difference which form is used as long as the designer pays particular attention to the form and uses the data accordingly. As a convenience, the series-parallel equivalent conversion equations are given in Appendix A.

For example, reading the complex input impedance, from Figures 1 and 2 at 50 MHz with 40 W output and a 12.5 Vdc collector supply, we obtain a value of 0.8 ohms resistance in parallel with a 500 pF capacitance.

Another form of impedance data presentation uses the series equivalent form plotted on a Smith Chart. This form is popular with UHF power transistors due to the extensive use of the Smith Chart in microstrip network synthesis. Figure 4 is an example of large-signal impedances plotted on a Smith Chart plot. Note that Figure 4 includes complete complex output impedance data, not just the output capacitance. This topic is discussed more fully in the section on collector load resistance.

AMPLIFIER DESIGN

After selection of a transistor with the required performance capabilities, the next step in the design of a power amplifier is to determine the large-signal input and output impedances of the transistor. When using devices for which the data is available, this step involves nothing more than reading the complex impedance values off of the data sheet. If only output capacitance is given on the data sheet, the collector load resistance may be calculated in the manner described in the Collector Load Resistance Section of this note.

Again, the designer is cautioned to carefully determine whether the data sheet impedance curves are in parallel or series equivalent form, and to use the data accordingly. If the data is not available, a later section of this note contains information on large-signal impedance measurement.

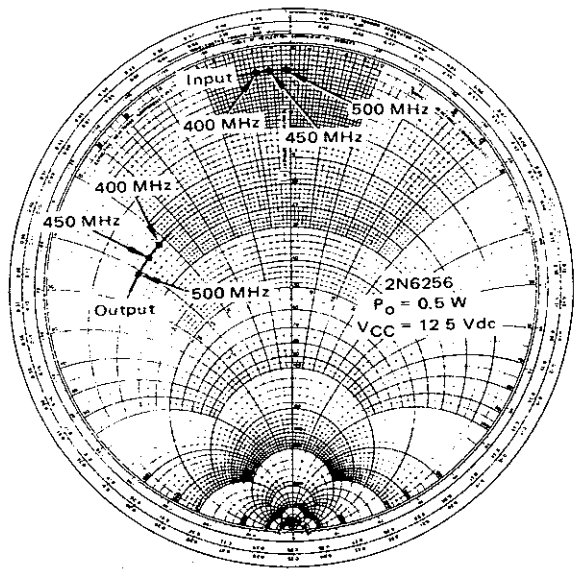


FIGURE 4 – Large Signal Input and Output Series Impedances, 2N6256

Having determined the large-signal impedances, the designer selects a suitable network configuration and proceeds with his network synthesis.

The primary purpose of this note is to describe the large-signal impedance concept. Accordingly, network selection and synthesis are beyond the scope of this discussion. For specific transmitter design examples using this concept, the reader is referred to the following Motorola Application Note: AN-548A.

COLLECTOR LOAD RESISTANCE

Large-signal impedance data at HF and VHF have for the most part been published by Motorola without collector load resistance information. The reason is that the load resistance can easily be calculated. The conditions necessary to obtain this load resistance derivation will now be discussed.

If certain simplifying assumptions are made, the theoretical collector voltage of a power amplifier with a tuned output network is a sine wave which swings from zero to 2 V_{CC}, where V_{CC} is the dc collector supply voltage. These assumptions include:

1. $V_{CE(sat)}$ is equal to zero.
2. The output network has sufficient loaded Q to produce a sine wave voltage regardless of transistor conduction angle.
3. The voltage drop in the dc collector supply feed system is zero.
4. The collector load impedance at all harmonics of the operating frequency is zero.

Obviously none of the foregoing assumptions is true, and the most serious discrepancies probably arise from assumptions 1 and 4. However, conditions are close enough to give good results.

Let us assume for a moment that this theoretical condition does exist. The parallel equivalent collector load resistance, R_L', then becomes a function of desired RF output power and V_{CC} only. The expression for R_L' given in equation 1 is readily derived.

$$R_L' = \frac{(V_{CC})^2}{2P} \qquad (1)$$

where P = RF output power

Therefore, the complex collector load impedance for an amplifier design would be the conjugate of the parallel equivalent output capacitance and collector load resistance computed with Equation 1.

Figure 5 provides a graphic solution to Equation 1 for the four popular dc supply levels of 12.5, 13.6, 24 and 28 volts.

Despite the assumptions required, experience with HF and VHF lumped-component, power amplifiers with supply voltages from 7 to 30 Vdc and power output levels from a few tenths of a watt to 300 watts have proven that the use of Equation 1 to compute R_L' for network synthesis yields good results. That is to say, the types of HF and VHF lumped component collector output networks which have proved best from the standpoint of proper impedance matching with low losses and smooth tuning generally have a sufficient tuning and matching range to compensate for any errors associated with Equation 1.

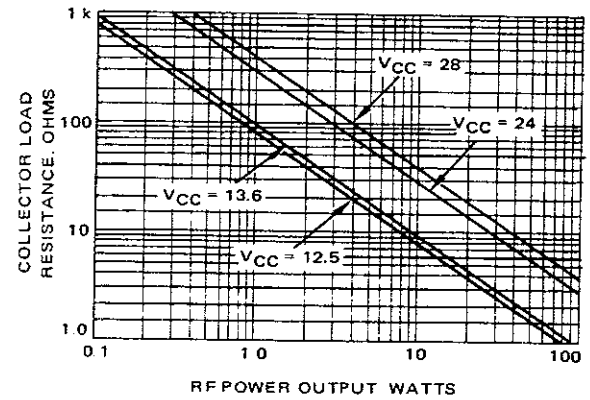


FIGURE 5 — Collector Load Resistance versus Power Output

Of course if the $V_{CE(sat)}$ of the transistor is accurately known for the frequency of operation and collector current swings anticipated in a particular amplifier, Equation 1 is readily modified as follows:

$$R_L' = \frac{(V_{CC}-V_{CE(sat)})^2}{2P} \qquad (2)$$

The advent of greatly increased numbers of UHF power transistors and their associated amplifier design problems brought some revisions to Motorola's methods of presenting large-signal transistor impedances for UHF devices. Among the reasons for this are the popularity of microstrip matching networks and the higher $V_{CE(sat)}$ values at UHF.

The major difference in the data format involves output impedance, which is presented in full complex form instead of plotting parallel equivalent output capacitance only and using Equation 1 to compute the load resistance. Further, the UHF devices are measured in a microstrip test amplifier for the purpose of determining the transistor impedances in an environment which is as close as possible to that of the majority of the actual applications of the device. And finally, a Smith Chart plot is used as this is more convenient to the microstrip network designer, who often makes extensive use of the Smith Chart as a design tool.

Future Motorola data sheets may also include collector load resistance data at frequencies below UHF. The information is automatically generated for the test circuit in use while measuring C_{in}, R_{in} and C_{out}.

PARAMETER MEASUREMENT

Although design engineers will find large-signal impedance characterization on Motorola data sheets for RF power transistors, it may help to know how this data is obtained. The transistor is placed in a test circuit designed to provide wide tuning capabilities. Design of the first

test amplifier for a new transistor type is based on estimates of input and output impedance.

Since the input and output impedances are needed to design an amplifier which is then used to measure the impedances of the device, we have a "chicken or the egg" type of problem. Wide tuning range networks help compensate for errors in the impedance estimates and they also permit the same characterization amplifier to be used at multiple power output levels.

The amplifier is tuned for a careful impedance match at both input and output. Several precautions are in order to insure that this is accomplished.

Tuning for maximum power output is valid only if the source and load impedances are an accurate 50 + j 0 ohms. Usually a good 50 ohm load is available in the laboratory. Such a load should be used, as tuning for maximum output power for a given input power is the best method to use on the amplifier output network.

The input network poses some additional problems. First, many laboratory RF power sources are not accurate 50 ohm generators. A generator impedance that is not 50 ohms can introduce errors in measuring gain as well as input impedances. In addition, a source with high harmonic levels can cause difficulties in low Q input networks.

A good solution to this problem is to use a dual directional coupler or directional power meter in the coax line between the generator and the test amplifier. The amplifier is then tuned for zero reflected power, thus indicating that the input network is really matching the transistor input impedance to 50 + j 0 ohms.

In practice, the reflected power usually will not null all the way to zero, so one should insure that the null is at least as deep as that obtained with a good 50 ohm passive termination.

In some cases, the amplifier will reflect enough harmonic power to prevent a satisfactory reflected power null from being obtained. A good solution to this problem is to place a fundamental frequency bandpass filter at the reflected power port of the dual directional coupler.

A typical test amplifier for HF and VHF measurements is shown in Figure 6. For UHF device characterization, amplifiers employing microstrip matching networks are most commonly employed.

After the test amplifier has been properly tuned, the dc power, signal source, circuit load, and test transistor are disconnected from the circuit. Then the signal source and output load circuit connections are each terminated with 50 ohms. After performing these substitutions, complex impedances are measured at the base and collector circuit connections of the test transistor (points A and B respectively in Figure 7). The desired data, the transistor input and output impedances, will be the conjugates of the base circuit connection and the collector circuit connection, impedances respectively.

By operating test amplifiers at several different frequencies with at least two power outputs, sufficient data can be obtained to characterize a transistor for the majority of its power applications.

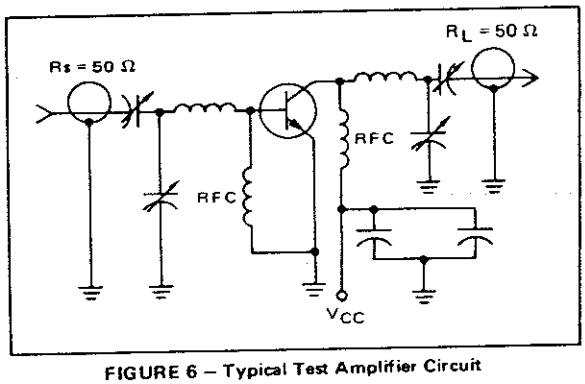
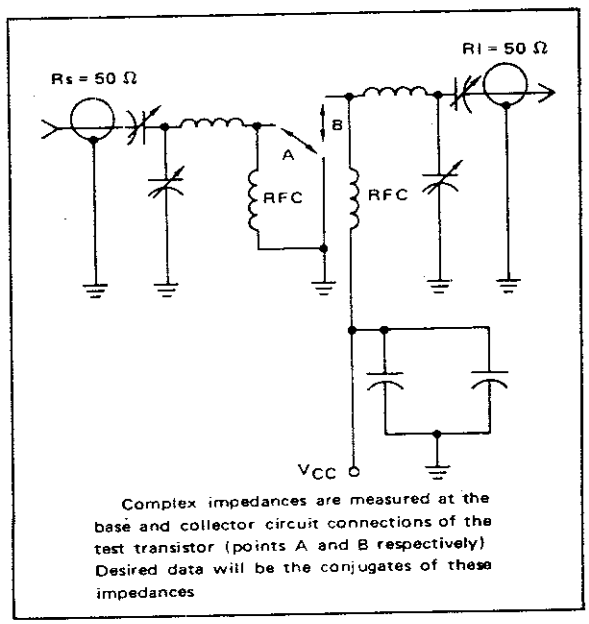


FIGURE 6 – Typical Test Amplifier Circuit



Complex impedances are measured at the base and collector circuit connections of the test transistor (points A and B respectively). Desired data will be the conjugates of these impedances.

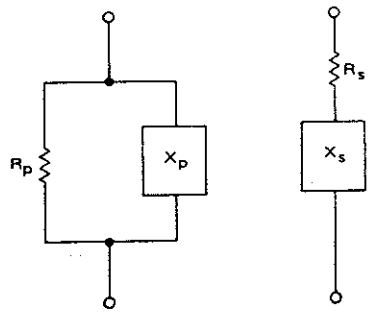
FIGURE 7 – Test Circuit with Transistor Removed

SUMMARY

The large-signal impedance characterization of RF power transistors has provided the most systematic and successful power amplifier design method the author has encountered since the concept was explored in depth in the mid 1960's.

APPENDIX A

PARALLEL-TO-SERIES AND SERIES-TO-PARALLEL IMPEDANCE CONVERSION EQUATIONS



$$R_p = R_s \left[1 + \left(\frac{X_s}{R_s}\right)^2\right]$$

$$X_p = \frac{R_p \cdot R_s}{X_s}$$

$$R_s = \frac{R_p}{1 + \left(\frac{R_p}{X_p}\right)^2}$$

$$X_s = \frac{R_s \cdot R_p}{X_p}$$