Class C Power

The primary concern of the RF transistor designer is meeting the requirements for output power, gain, and ruggedness at the specified frequency and supply voltage.

Most RF applications typically require 12.5 or 28 volt operation of a power device in a mobile transmitter, base station, or avionics application. This choice dictates the epitaxial layer resistivity. Low resistivity, about 1 ohm/cm, is used for mobile devices, while 28 V base station and avionics devices are usually built using epi with 2 ohm/cm resistivity. Epi resistivity controls collector breakdown voltage, since the resistivity value determines the maximum possible breakdown voltage. Typically, a particular device rarely achieves this bulk breakdown value because of junction curvature and surface effects. When high voltages are present in an amplifier, high breakdown voltages are needed if the transistor is to survive. High voltage breakdowns are usually obtained by such added features as collector depletion rings, or by a high voltage diffusion surrounding the relatively shallow RF base diffusion. Voltages in excess of 150 volts are easily obtained this way.

Output power is determined primarily by the "electrical size" of the chip. Two common methods of sizing are emitter diffusion periphery and base diffusion area. Emitter periphery sizing is based on the premise that there is some optimum current which should be injected for each mil of emitter periphery. The base area sizing is based on an optimum power density. Both of these techniques are oversimplifications which make it impossible to apply them to widely varying device geometries and applications. Motorola uses a different method of sizing based on each geometry's Current Factor. Current Factor values are obtained by considering both emitter periphery effects and power density. Proper weighting of both factors makes this technique of sizing widely applicable. No matter what sizing technique is chosen, the end result is that greater power-handling capability requires larger chips. Small-signal devices, with only a few milliwatts of output power, and large devices with 100 watts output, range from current factors of only 1 to nearly 2000.

An alternative approach to high output power is to use several smaller chips in parallel. Unless extreme care is taken, this approach can result in unequal current and power sharing. Single large chips are also susceptible to this sharing problem unless specific steps are taken to ensure even current distribution. The primary method of handling this problem is by the use of well-designed emitter resistor layouts. The lowest value of emitter resistance on a chip is chosen to prevent thermal runaway up to the highest temperatures the device may encounter, possibly up to 300°C during output impedance mismatch conditions. An appropriate matrix of emitter resistance values is constructed so that the overall current distribution among the many parallel emitter sites results in an even thermal distribution. Verification of thermal balance is obtained by precise infrared microscope measurements across the entire chip.

The thermal balance of larger chips is also improved considerably by "cell spreading." In this techique the base diffusion area is broken up into smaller areas, or cells, and each cell is sufficiently removed from those adjacent to eliminate thermal interaction. The net effect is to achieve lower thermal resistance. This is exceedingly important in large devices where high power dissipation levels can cause excessive junction temperature when thermal resistance is not minimized. Some symptoms of excessively high temperature operation are low efficiency, power slump, and, frequently, total device failure.

The overall ruggedness of a transistor is enhanced by many techniques. All of them are aimed at preventing two things: junction breakdown due to excessive voltages and failure due to hot-spotting. Here again, epitaxial layer resistivity and thickness are used to alter breakdown voltages and saturated output power. Thermal balancing by base cell spreading and using emitter resistors also has a strong effect on ruggedness. These techniques are commonly referred to as collector and emitter ballasting. Ballasting of either type can improve ruggedness for a fixed geometry size (current factor), but there is a definite trade-off with gain. Usually increasing ruggedness requires decreasing gain unless one is willing to pay the penalty of the cost of larger die.

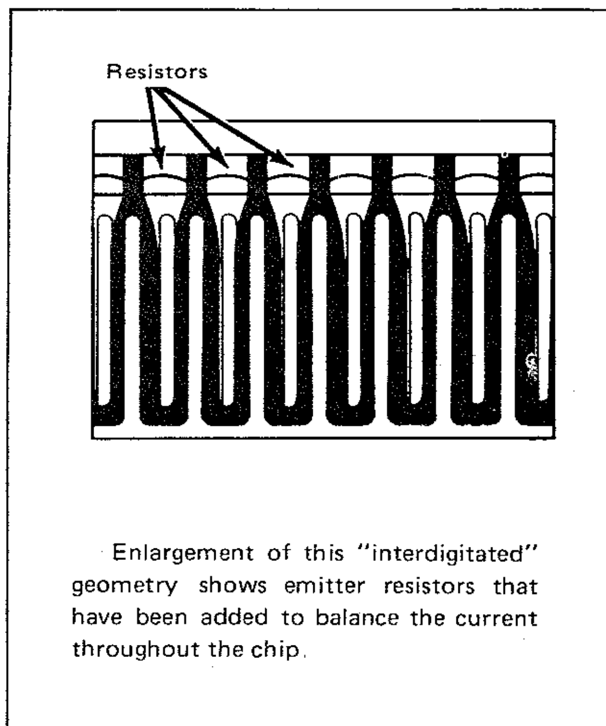
Large die can also adversely affect gain, since it is a practical fact that gain decreases by 2 dB for each doubling in current factor. To offset this gain decrease, the designer has another technique available—increase the packing denisty within the chip. The most common method of measuring packing density is with the figure of merit obtained from the ratio of emitter periphery (E_P) to base area (B_A) of the chip. Higher E_P/B_A ratios result in higher gain. Typically, E_P/B_A ratios are as shown in the table.

Ep/B_A	FREQUENCY	GEOMETRY TYPE
0.5–1.5	3-30 MHz	Interdigitated
1.5–3.5	VHF	Interdigitated or Spine (Overlay)
3.5–4.5	UHF	Spine (Overlay) or Mesh (Network)
5.5–6.5	800-900 MHz	Mesh

Higher Ep/B_A ratios generally mean greater processing difficulties. These difficulties are somewhat offset by the choice of geometry type. Fundamentally, the interdigitated geometry requires narrow spacing between emitter and base fingers and narrow finger widths. The maximum Ep/B_A ratio obtainable with an interdigitated structure of uniform spacing "S" is given by

$$(Ep/B_A)\ MAX = \frac{0.45}{S}$$

Spacings of 0.08 mil are the minimum easily obtainable with current technology, giving a maximum figure of merit of 5.6. Actual devices with this spacing are usually about 4.5. Building a large power device using this geometry calls for a great many narrow metallization fingers.



Enlargement of this "interdigitated" geometry shows emitter resistors that have been added to balance the current throughout the chip.

This approach increases the probability of a metallization defect linking adjoining fingers and enhances failures due to metal migration. The spine or mesh geometries used for higher figure of merit do not completely relieve the tight spacing requirements. In both cases, tight metal spacing is relieved while diffusion spacings are not. For example, 4.5 is the maximum Ep/B_A ratio for a 0.1 mil spacing with an interdigitated device. Motorola's family of UHF power devices MRF641 (15 watt), MRF644 (25 watt), MRF646 (45 watt), and MRF648 (60 watt) are constructed using a split mesh (adjoining emitter fingers are not interconnected). All four devices have an Ep/B_A ratio of 4 and are built with a 0.1 mil spacing between adjacent emitter and P+ diffusion areas. Similar tight spacing is required in the mesh geometry used for the 800-900 MHz 7, 20, 30, and 40 watt devices. Here the spacing is reduced to 0.06 mil, using a mesh geometry. Without tight spacing of emitter to P+ such as these devices have, high Ep/B_A ratios will not produce good gain. The introduction of the P+ is required to maintain full utilization of all elements of the emitter periphery. Introducing undulations in the shape of the emitter to increase the periphery without a closely spaced P+ will cause some elements of the periphery to be debiased due to uneven base voltage drops.

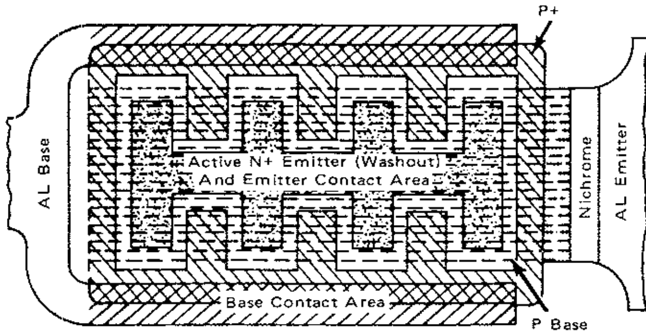
The metal migration failure rate as measured by MTBF (Mean Time Before Failure) depends on current density, metallization cross-sectional area, and activation energy. Activation energy may be varied by the choice of metallization with gold and aluminum being the two most common choices. Motorola uses gold metallization for both avionics and 28 volt base station devices where continuous operation is anticipated. Mobile devices are usually constructed of aluminum. In either case, devices are designed for a minimum of 10 years MTBF

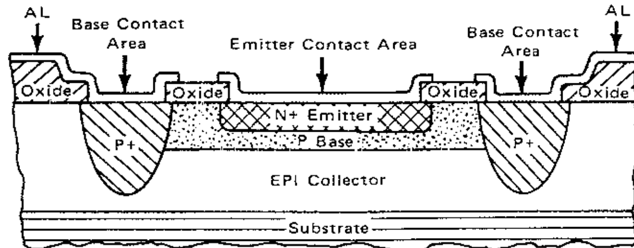
Linear Power

Linear operation is usually accomplished by building the same type of transistor structure as used in Class C operation. The major difference is the linearity requirements force the use of devices with larger current factors. They are also usually fabricated with slightly lower collector resistivity. The combination of these factors allows the device to maintain good linearity with high power output levels. Motorola has led the industry with its family of SSB large-chip transistors, MRF421, MRF422, MRF428. These chips are large, 140 X 250 mils, and have Current Factors approaching 2000. The higher voltage devices are built using a combination of both depletion rings and deep P+ high voltage diffusions. All feature thermal ballasting through emitter resistor matrices.

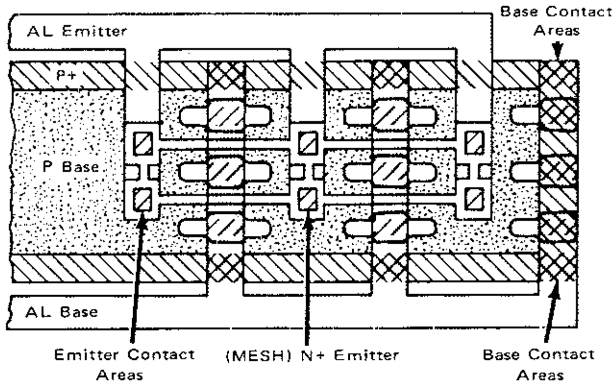
Small Signal

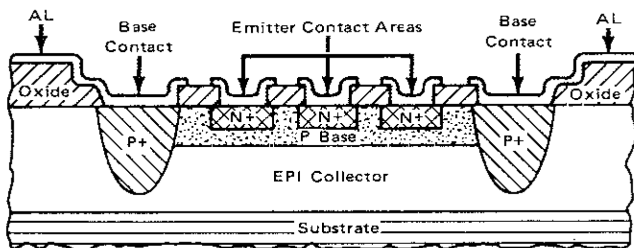
Small-signal devices are constructed from the same types of geometries as used for power devices except on a much smaller scale of Current Factor. The small geometries do not suffer from the gain reduction due to size, allowing the use of lower Ep/B_A ratios for equivalent gain.





Overlay Structure. Individual emitter cell blocks are diffused into a common base region Emitter interconnection runs are made over a passivating silicon dioxide layer, reducing the need for critically thin interdigitated metal fingers





Network Emitter Structure. This structure maximizes emitter periphery to base area ratio but pays for it with increased production difficulty and increased contact resistance

Motorola employs a thin nichrome barrier (not shown) between the silicon and the aluminum metalization in most network emitter and overlay devices to prevent aluminum metal migration thus improving long-term reliability.

Quite commonly, small-signal transistors are not only required to have a minimum gain, but also a minimum f_t This parameter is a measure of the total emitter-to-collector transit time As the collector current is increased, the value of f_t increases initially, peaks, and then finally decreases. The peak value is determined by the base and emitter region transit times This parameter is controlled by both the base junction depth and the emitter doping species. Using conventional diffusion processes with a single base and emitter diffusion, maximum achievable f_t for NPN transistors is about 3–4 GHz without severely degrading the normally desirable dc characteristics, namely BV_{CEO} and h_{FE}.

The logical solution is to use arsenic as the emitter dopant species. Arsenic has an advantage over the more commonly used phosphorus diffusion source. The concentration dependent diffusivity of arsenic causes a very abrupt emitter profile. The increased profile gradient reduces the storage of free carriers in the emitter space charge layer, reducing the layer transit time, and increasing f_t. Unfortunately, arsenic diffusion technology is difficult at best.

The simplest method for using arsenic as a dopant species is to implant it. Motorola has introduced a whole family of implanted arsenic emitter NPN transistors These devices have typical f_t of 6 GHz without sacrificing dc characteristics.

A family of low noise devices has also been fabricated using similar processes Low noise figure (NF) places additional requirements on both f_t, the doping density of the base under the emitter, and the emitter diffusion width Through special controlled processing, excellent NF values are obtained in the 1 to 2 GHz region. This performance requires high f_t, low base spreading resistance, and 0.05 mil wide arsenic implanted emitters.