TRANSISTOR CHARACTERISTIC PLOTTING

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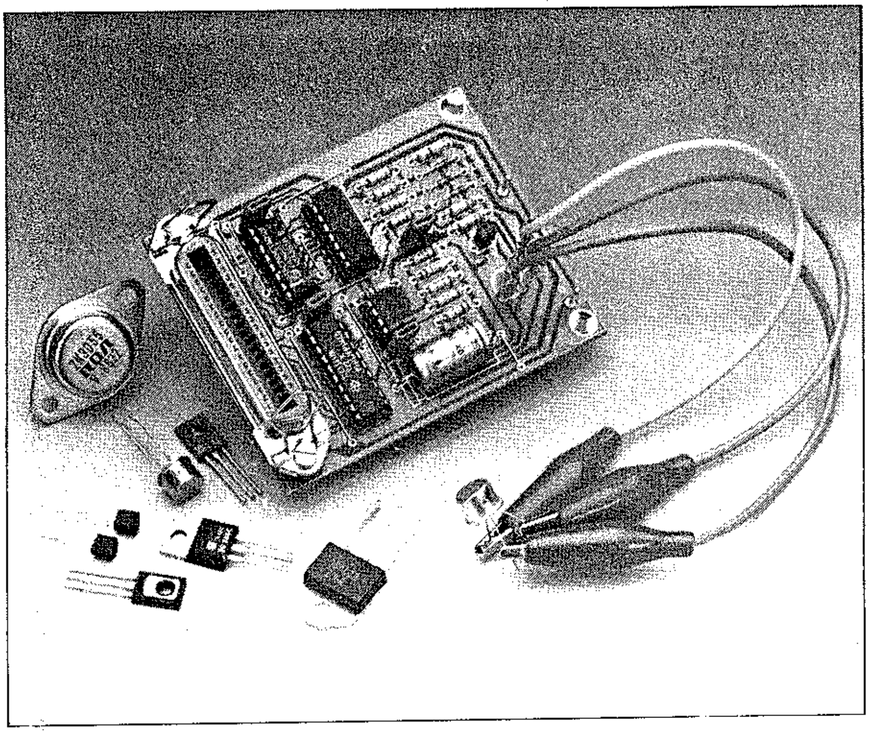
The circuit described here makes use of a computer to plot the so-called output characteristic and determine the small-signal current gain, h_{fe}, of an n-p-n transistor. These two transistor parameters are of great importance for classifying an unmarked transistor, for a reliable good/faulty test, and for selecting matched transistors from an available lot. Although the program that controls the circuit is written for the Atari ST series of home computers, the use of the Centronics port should enable owners of other micros to adapt their own version fairly easily.



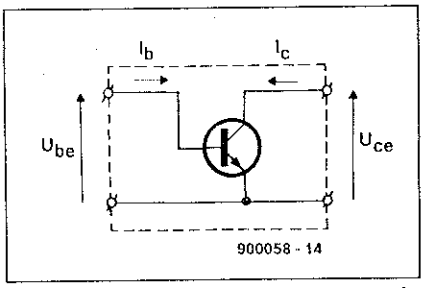


Fig. 1 Transistor in a four-pole test circuit.

The use of a computer and a printer, instead of the more usual oscilloscope, to measure and record transistor parameters is subject to one important proviso: the transistor under test must be located between a digital-to-analogue converter (DAC) and an analogue-to-digital converter (ADC). The circuit presented here has, therefore, a digital input as well as a digital output, both of which are connected to the Centronics (parallel) printer port to convey the necessary data and control levels to and from the computer.

Transistor parameters

Since the basics of transistor characteristic plotting have been covered relatively recently in Ref. 1, only a recap is given here.

Figure 1 shows an ideal transistor in the standard four-pole test circuit in which voltages are applied to the base-emitter junction and the collector-emitter junction.

The first important transistor parameter that may be obtained from this basic test circuit is the so-called output characteristic, which is a curve that describes the relation between the collector-emitter voltage, U_{CE}, and the collector current, I_C, with the base current, I_B, as a parameter. Ideally, such curves are straight lines since the collector current is determined by the base current only, and not by the collector-emitter voltage. In practice, however, the so-called early effect causes the I_C-vs-U_{CE} characteristic to become a curve rather than a straight line, particularly at relatively low values of U_{CE}.

The second important characteristic is the small-signal current gain, h_{fe}. This is defined as the ratio of change in collector current, δI_C, to the change in base current, δI_B, that produces it, when the collector-emitter voltage is kept constant:

$$h_{fe} = \delta I_C / \delta I_B = I_c / I_b \text{ when } U_{CE} \text{ is constant.}$$

Most transistor manufacturers provide this parameter at two or three values of U_{CE} and I_B.

The present circuit plots the output characteristic of n-p-n transistors for eight values of I_B, and in addition automatically calculates a statistically derived h_{fe} value. With these two parameters on the screen and on paper (hard copy from the printer) you are in a position to select matching transistors for critical applications, or find a substitute for an unknown transistor.

Circuit description

As already stated, the transistor under test (TUT) is located between a DAC (IC2) and an ADC (IC1) —see Fig. 2. All control and processing of measured values is carried out by the computer.

The circuit uses two supply voltages: 5 V for the DAC, the ADC and counter IC1, and 15 V for the transistor test circuit and the associated voltage amplifiers. The higher supply level of 15 V is required to provide the TUT with a maximum collector-emitter voltage of about 9 V.

The measurement is cyclic and controlled by the computer. First the base current of the TUT is set at a certain value. Next, the collector-emitter voltage is raised gradually from 0 V to about 9 V, and the resulting collector current is measured. This process is repeated with the next higher value of the base current. The step size is 25 µA and there are eight steps starting at I_B = 0 µA. The test cycle is complete at I_B = 175 µA.

The control program provides a stream of clock pulses on the D1 (data-1) line of the Centronics port. The clock pulses are counted by IC_1, a Type 74HCT4040. The counter values at the Q0–Q7 outputs are converted to an equivalent analogue voltage between 0 V (value: 0) and 2.5 V (value: 255) by DAC IC_2. The Q8, Q9 and Q10 outputs of IC_1 control the base current of the TUT in 8 steps. The required current step size of 25 µA is obtained with the aid of resistors R_3–R_6. Note that the value or equivalent value of each resistance at the three counter outputs is derived from 180 kΩ, since this value results in a current flow of about 25 µA at a logic high voltage of about +4.8 V at the respective counter outputs.

The clock pulses provided by the computer cause the voltage at the output of IC_2 to be increased from 0 V to the reference voltage of the ZN425 (2.5 V) in 255 steps. Initially, this happens with Q8, Q9 and Q10 of the counter being low so that I_B = 0 µA. The analogue voltage is amplified by a factor of four by opamp IC_{3a}. The resulting voltage range at the collector of the TUT is about 0 V to 9 V. This voltage range is divided by two by R_{15}-R_{16} to prevent the maximum input voltage of ADC IC_4 being exceeded.

The emitter current of the TUT causes a voltage drop across R_{14}. This voltage is amplified by a factor of 48 by opamp IC_{3b} before it is applied to the A0 input of the ADC. Note that the emitter current rather than the collector current of the TUT is measured. This can be done without problems, however, since in the four-pole test circuit the emitter current is the sum of the collector current and the base current. The latter is in the µA range and is therefore negligible with respect to the collector current, which is in the mA range.

Every time U_{CE} of the TUT reaches its maximum value of about 9 V, it is reset to 0 V again, and the base current is increased by 25 µA, to start a new curve

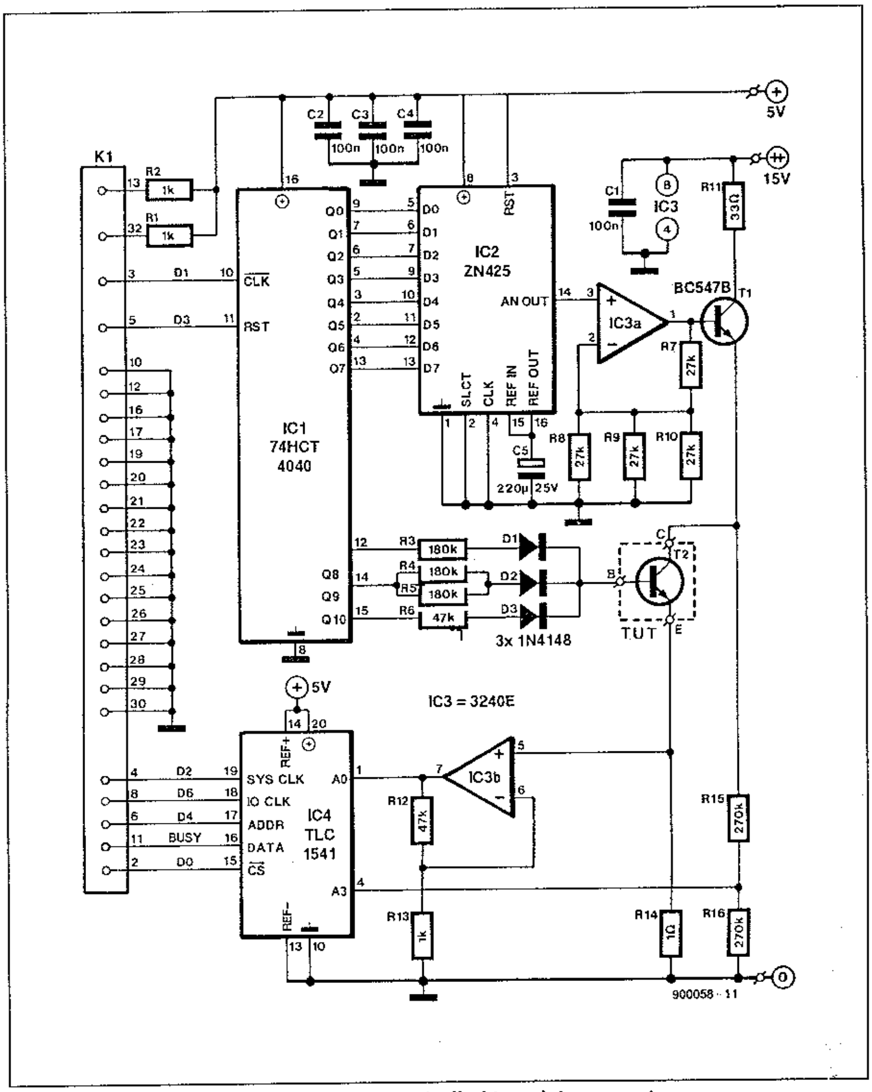


Fig. 2. Circuit diagram of the computer-controlled transistor curve tracer.

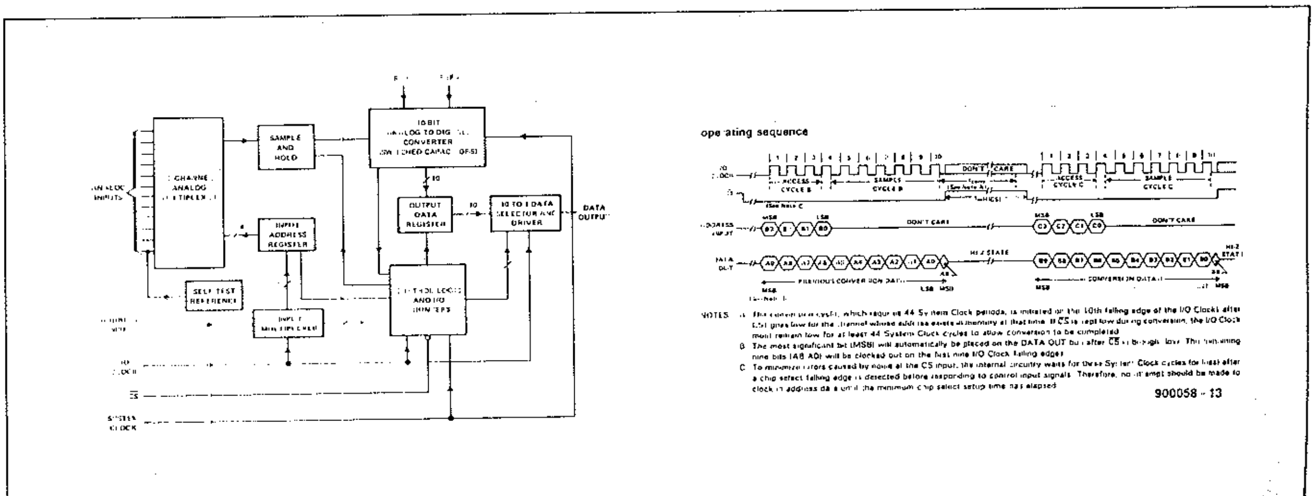


Fig. 3. Block diagram of the TLC1541 and the pertinent pulse timing on which the control program flow is based (*illustration reproduced by kind courtesy of Texas Instruments*).

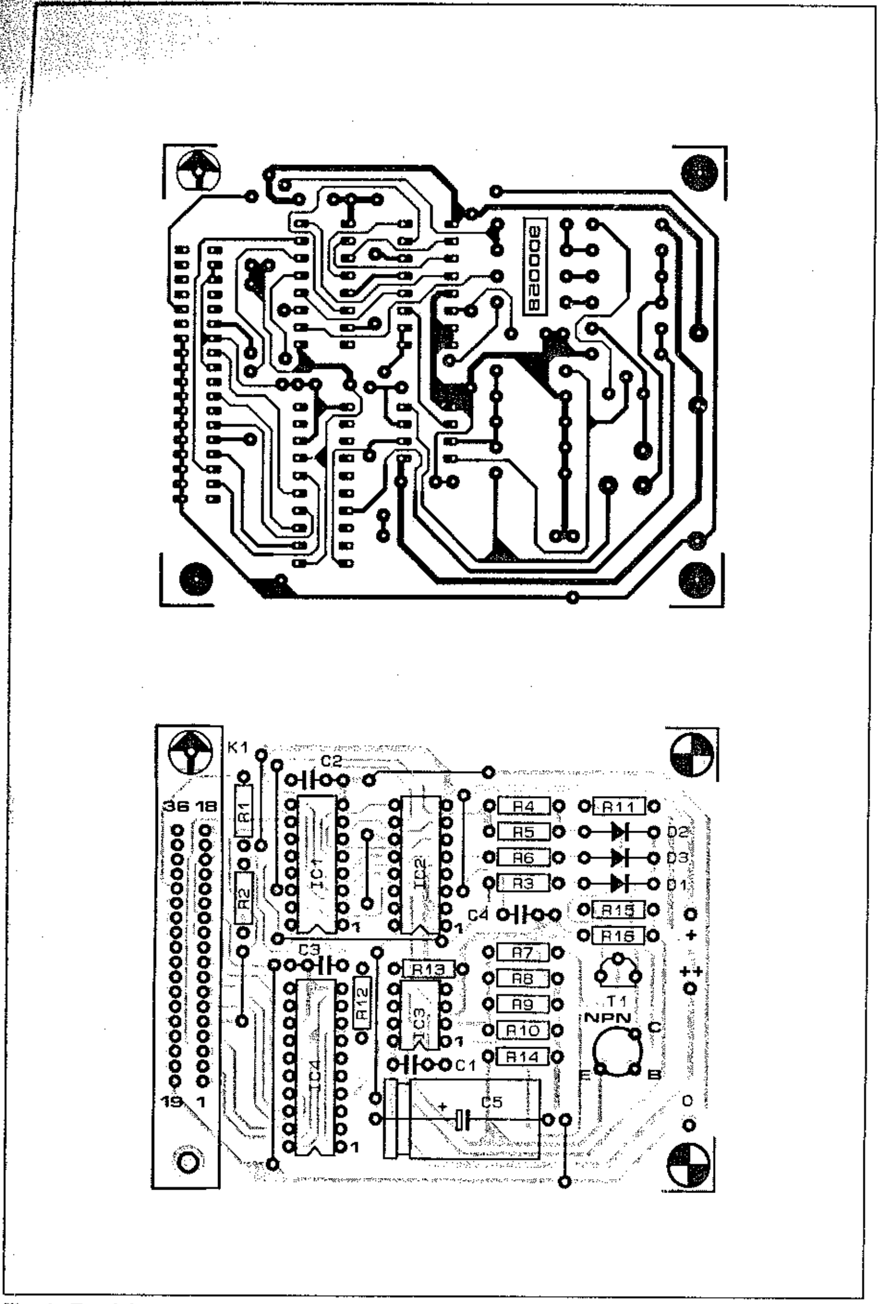


Fig 4 Track layout and component mounting plan of the single-sided printed-circuit board

COMPONENTS LIST

Resistors:		
3	1k0	$R_1;R_2;R_{13}$
3	180k	$R_3;R_4;R_5$
2	47k	$R_6;R_{12}$
4	27k	R_7–R_{10}
1	33Ω	R_{11}
1	1Ω0	R_{14}
2	270k	$R_{15};R_{16}$
Capacitors:		
4	100n	C_1–C_4
1	220µF 25V	C_5
Semiconductors:		
1	BC547B	T_1
1	74HCT4040	IC_1
1	ZN425	IC_2
1	CA3240E	IC_3
1	TLC1541	IC_4
3	1N4148	$D_1;D_2;D_3$
Miscellaneous:		
1	36-way PCB-mount Centronics socket	K_1
1	PCB	900058
1	control program	ESS1431

This cycle is repeated eight times until a high pulse on Centronics line D3 resets counter IC_1.

Processing the analogue quantities

The Type TLC1541 (IC_4) from Texas Instruments is a 10-bit, 11-channel analogue-to-digital converter with an internal analogue multiplexer and a serial data output. In the present circuit, only two of the available 11 channels are used. One channel, A0, takes the I_C parameter, the other, A3, the U_{CE} parameter.

Figure 3 shows the block diagram of this interesting LinCMOS chip, along with the pertinent timing sequence.

The computer selects the channel from which it requires the 10-bit data. This selection is accomplished by pulling $\overline{CS}$ of the TLC1541 low via Centronics bit D0 and applying the relevant channel code (0 or 3) serially via Centronics bit D4. All channel selection, timing, conversion, and serial data output operations in the TLC1541 run under the control of SYSCLOCK and IO CLOCK, for which the required pulses are supplied by the computer via Centronics lines D2 and D6 respectively.

The 10-bit output data for processing by the computer is shifted out serially with the MSB first. The conversion error of the TLC1541 is ±1 LSB, or 5 V/1024 = 4.8 mV at a maximum voltage of 5 V at the channel inputs. Hence, the maximum error of U_{CE} is about 10 mV, which is acceptable in the present application. The computer reads the measured value by monitoring the state of the BUSY input line on its Centronics port.

Control program

The control program for the curve tracer must:

- provide clock pulses to the U_{CE}-I_B generators
- arrange the timing sequence of the TLC1541
- read the measured values of U_{CE} and I_C that belong with a particular value of I_B.
- calculate an average h_{fe} value
- plot I_C as a function of U_{CE} with I_B as a parameter
- provide a graphics screen
- allow the graphs on the screen to be dumped to a printer to obtain hard copy

All this is arranged by a program written in C for the Atari ST series of computers. This program, npn.prg, and the source file, npn.c, are available on disk. A few examples of output characteristic plots are shown in Fig. 5.

Construction and use

Construction of the computer-controlled curve tracer is straightforward if the printed-circuit board shown in Fig. 4 is used. Connector K_1 is a standard 36-way Centronics socket for PCB mounting. As shown on the photograph of our prototype, this connector is mounted on two plastic PCB spacers. An alternative that does not require spacers is a similar connector with angled terminals. Both types of connector are often referred to as 'blue-ribbon' and are commonly used on matrix printers.

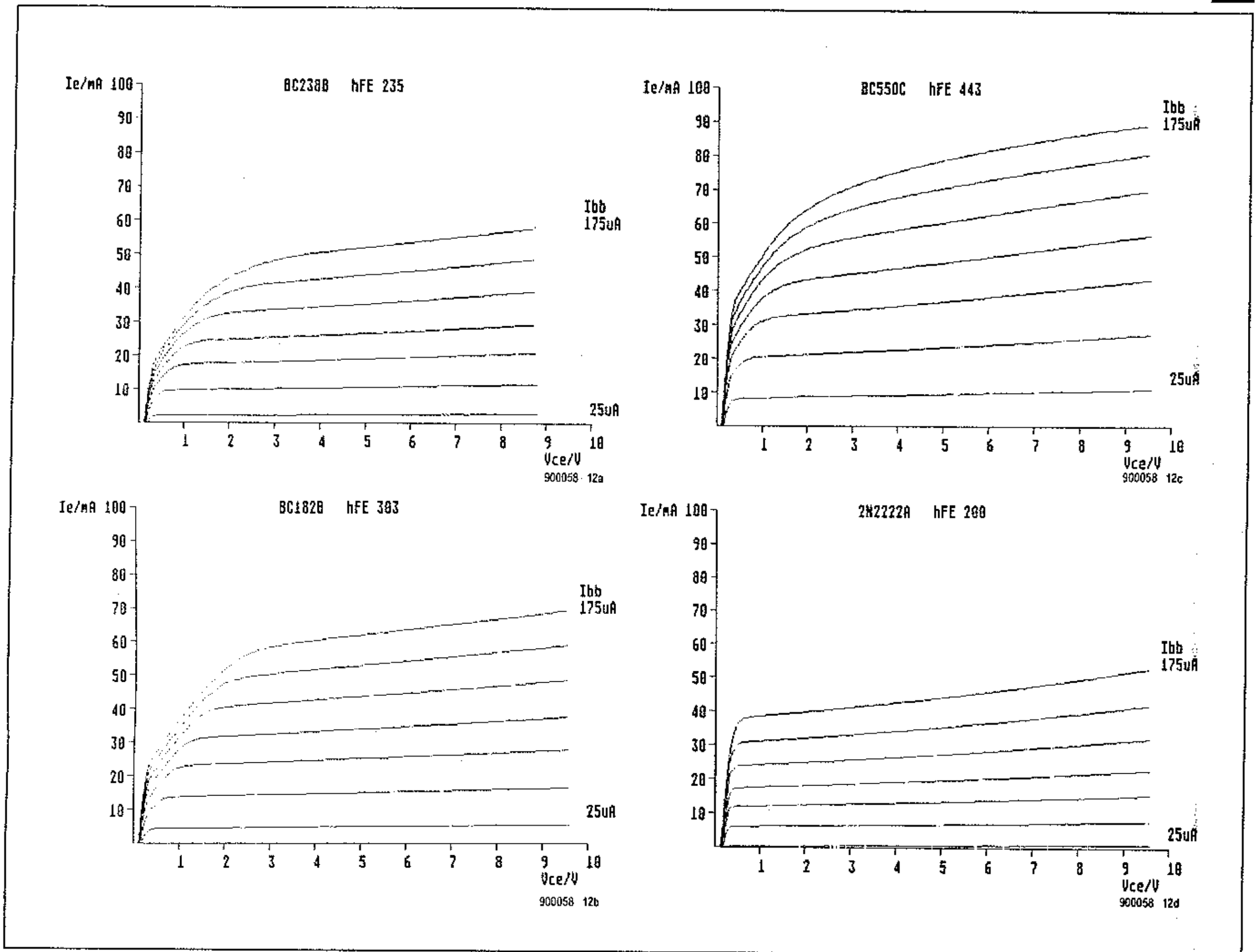


Fig. 5. A few examples of plots made by the program

Start the construction by fitting the seven wire links, followed by the IC sockets. Next, mount the resistors, the capacitors, diodes and the single transistor.

A transistor test socket may be used for inserting the TUT, but in many cases three light-duty flexible wires with small, plastic covered crocodile clips are perfectly all right.

The ICs are fitted last. Observe their orientations, and be extra careful with the ZN425 and the TLC1541!

The circuit requires a separate power supply that provides regulated output voltages of 5 V (+ terminal) and 15 V (++ terminal). The current requirement for the 5-V supply is only 50 mA or so, while that of the 15 V supply is determined mainly by the collector current of the TUT. In most cases, 200 mA will be adequate. Voltage regulators such as the 7805 and the 7815 are fine for these applications, but do not forget the usual decoupling capacitors to prevent noise and oscillation.

The completed PCB is fitted in a suitable ABS enclosure, the size of which depends on whether the power supply is internal or external. In any case, do not use mains adapters to power the circuit, since these do not in general provide the required output voltage stability.

The curve tracer is connected to the computer by a standard printer cable.

The curve tracer is simple to use: insert or connect the transistor under test (make sure you get the b-c-e terminals right), apply power and run the control program by clicking twice on 'npn prg' in the file menu. The program, after being loaded, will prompt you to enter the transistor type and type any key to start plotting. Do not worry if nothing appears to happen at first, since the $I_B = 0$ µA curve is drawn first. Once the output characteristic appears complete on the screen, the program halts and waits for a key to be pressed to take you back to the file menu. Hard copy may be obtained before exiting the program by disconnecting the tracer from the printer port, connecting the printer, switching it on line and pressing the ALTERNATE and HELP keys simultaneously. Finally, the circuit and the program are suitable for testing n-p-n transistors only. The control program supplied on disk is suitable for **monochrome Atari ST** systems only. ■

Reference:

1. Transistor curve tracer. *Elektor Electronics* October 1988.