Designed to reduce jitter in a digital video disk measurement system, Chris Hancock's precision integrator achieves a repeatability of 0.1% on successive ramps at very high speeds.

Fast and precise integrator

I designed this precision analogue integrator to produce linear dV/dt voltage ramps clamped between +1.5V and −1.5V. The output ramps were produced from the edges of data pulses with a width of between three and fourteen multiples of a data clock running at 27MHz.

Rise and fall times of the data-pulse edges are symmetrical, with a typical value of 1.5ns. The linear slope of 3V, i.e. ±1.5V, is produced in a nominal time of 24ns. This is achieved using a novel feedback loop system, which makes use of state of the art 1.2GHz bandwidth operational amplifiers and 274MHz bandwidth clamp amplifiers.

Results show that the circuit can be used to produce linear precision clamped voltage ramps from the edges of the data pulses, whose widths are changing randomly over the entire range. Repeatability measurements indicate that it is possible to achieve a repeatability of 0.1% on successive ramps.

Background

The motivation designing this integrator came from the need to measure timing jitter between signal data and a synchronised data clock in a digital video disk measurement system. The data clock was running at 27MHz with a 1:1 mark-space ratio, and the width of the data pulses was between three and fourteen clock cycles, i.e. 111ns to 518ns. Voltage levels for both clock and data signals was ttl.

The rise and fall times of the data pulses were symmetrical, with typical values of 1.5ns. For the purpose of this work, the data pulses can be considered as being generated continuously, with random width between three and fourteen clock cycles.

We needed to produce a precision dV/dT ramp from the edges of these data pulses, and from this, voltage levels were to be sampled to enable the timing jitter between the rising edge of the clock and the data signal to be calculated.

Voltage levels taken from the ramp were fed into a fast eight-bit Phillips *TDA8703* a-to-d converter and stored in an *IDT7201* first-in-first-out memory, ready for subsequent processing. This article concerns only the analogue integrator.

We wanted the measurement system to run continuously, so it was vital that no charge remained on the integration capacitor at the start of the next signal integration. In addition, the clamped levels needed to be identical for each data pulse width.

Because we needed identical clamped levels, a basic active integrator using a single operational amplifier with a feedback capacitor was not an option. We needed a solution whereby the output from the integrator would remain constant at either the positive or negative clamp amplitude level for a predetermined time after the ramp level has changed between clamping voltage rails, ready for the next data edge to arrive.

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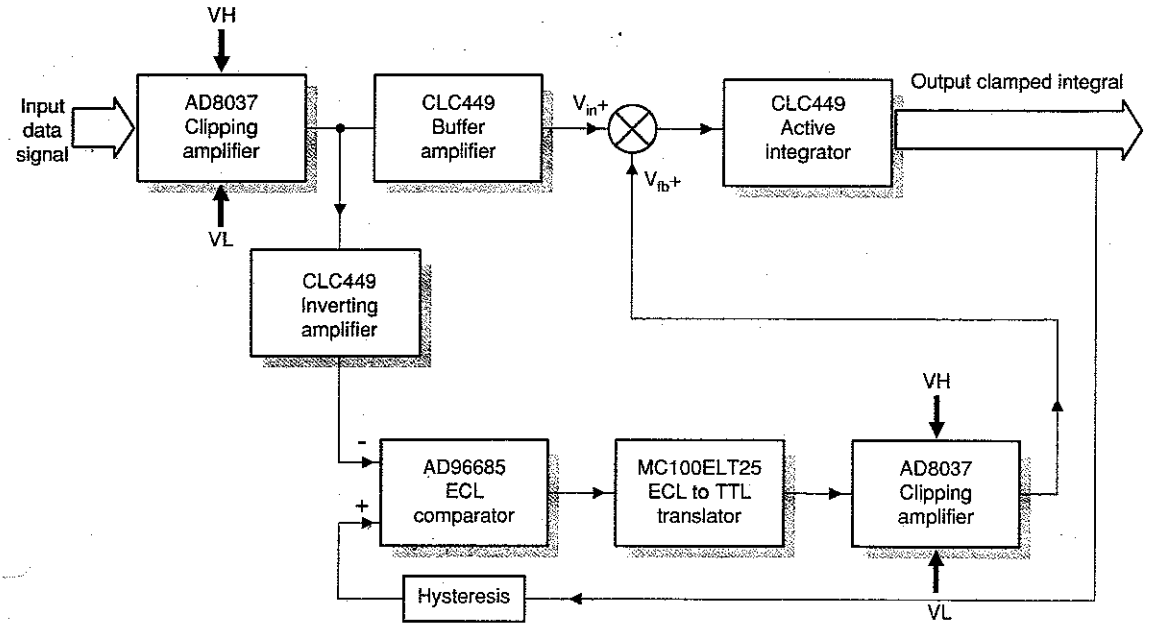

Fig. 1. Fast integrator in outline. Unlike other integrator designs, this one compares an inverted version of the clamped data pulse to a ramp level produced from a basic CR integrator. This CR integrator's forward input comprises the clamped version of the incoming data pulse. Comparator output is again clamped and then summed with the integrator's forward input.

When the integrator is used in the complete measurement system, the contents of the a-to-d converter can be interrogated at any time using an on-board digital signal processing system. After interrogation, the contents of the a-to-d converter, and hence the first-in-first-out memory, would be cleared, ready for the next level to be fed in. This means that the integrator should be running continuously, and since the width of the data could be between 111ns and 518ns, in 37ns increments, the integrator must be able to clip between +1.5V and -1.5V with a ramp time such that a timing jitter error can be accurately discerned from the ramp.

The ramp was designed to be 24ns long; this aspect of the design is detailed later. Since, theoretically, the maximum time that the level is to stay constant –i.e. 'held' – is 494ns, or 518ns–24ns, the level of voltage change during this time must be negligible. In other words, the level must be held constant at either the positive or negative clamp level.

Also, slope and measurement errors, due to temperature variations and delays through the active devices used in the feedback loop, had to be removed by carrying out a system calibration routine before each measurement run. Basically, this involved a fixed delay being introduced in the data clock signal, i.e. a clock skew, to compensate for the delays, together with an additional delay to ensure that the measurement is taken on a truly linear region of the ramp.

Circuit details

This integrator uses a novel method whereby the inverted version of the clamped data pulse is compared to a ramp level produced from a basic *CR* active integrator. This integrator's forward input consists of the clamped version of the incoming data pulse.

Comparator output is again clamped and then summed with the forward input of the integrator. From `Fig. 1`, you can see that the incoming data signal is first clamped using an Analogue Devices *AD8037* low distortion, wide bandwidth voltage feedback clamp amplifier.[1] This device conditions the input data signal to provide precise ±1.5V drive levels by setting up a closed-loop gain of 2 and then multiplying this by precise input voltage reference clamp levels, V_H and V_L.

These reference levels were derived from a National Semiconductor *LM368* precision 2.5V voltage reference, and a potential divider network, buffered using an National Semiconductor *LM358* quad operational amplifier.

At this point, the clamped data signal is split into two paths; one feeding a buffer amplifier, which consists of a Comlinear *CLC449* 1.2GHz ultra-wideband operational amplifier[2] configured to have a closed-loop gain of 6. Output from the buffer feeds one of the summing inputs to the active *RC* integrator, which again uses a *CLC449*.

In the other signal path, the clamped data signal is first inverted to provide a gain of –1 using a further *CLC449* and then fed into the negative input of an Analogue Devices *AD96685* ultra-fast comparator.[3] The positive input to the comparator is taken from the output of the active integrator.

Some hysteresis is introduced in this path to prevent changeover uncertainties from occurring. Output from the comparator is then translated from its ecl level to ttl, using a Motorola *MC100ELT25* translator[4]. the resulting signal feeds a second *AD8037* clamp amplifier, which is configured identically to the first clamp amplifier.

Note that we used an ecl comparator because it is the fastest device available for comparing two signals and changing the output state – even with the translator stage included.

Input clamp levels V_H and V_L are derived from the same precision voltage reference circuit as that used for the first clamp amplifier. The signal from the second clamp amplifier is then summed with the clamped and buffered version of the initial data signal at the input of the active integrator; hence closing the feedback loop.

If you assume that the two summing resistors are balanced and the clamp voltages are identical, then the output from the active integrator, with the loop closed, will ramp up or down, depending on the input voltage polarity. When the two voltages are 180° out of phase – i.e. inverted – the output clamped voltage is held and remains constant.

Figure 2 illustrates the operation of the circuit in terms of timing sequences. The first waveform shows the input data after it has been precision clamped. The ramp output from the active integrator is shown in waveform 2, which is compared with the inverted version of the clamped data, waveform 3.

When the ramp's amplitude reaches the inverted data input level, the output from the comparator, waveform 4, changes state. This signal is then conditioned by the second clamping amplifier, waveform 5, and added to waveform 1 to hold the output level constant at either the positive or negative clamp voltage levels.

Putting it into practice

The whole circuit, **Fig. 3,** was laid out on a multilayer board. Layer 1 contains the signal tracks, layer 2 the ground plane and layer 3 the power supply tracks.

All signal tracks were kept less than 3cm long, i.e. less then the wavelength of the highest possible frequency component contained in a data pulse. Power supply decoupling capacitors were placed as close as possible to the power pins; tantalum capacitors were used for the polarised values since these offer the lowest series resistance.

Surface mount capacitors and resistors were used throughout the design to minimise lead inductance. We ensured that low impedance power tracks were kept as far away as possible from sensitive device inputs to prevent the formation of leakage resistors, which can result in leakage currents often of higher magnitude than the device bias currents.

The devices were mounted directly onto the circuit board, since the extra inductance introduced by IC sockets is significant when operating at such high frequencies.

Resistors of 100Ω were placed in series with the output of the *AD8037* and *CLC449* devices to prevent oscillation and overshoot from occurring. Also, 50Ω termination resistors were used at the inputs to prevent pulse reflections and ringing.

The incoming ttl level data signals were ac coupled, using a 100nF ceramic capacitor, C_{60}. This enabled the signal to swing positive and negative around zero to enable it to reach the precision clamp levels, V_H and V_L. Resistor R_9 provides a dc path for bias currents; this prevents C_{60} from charging up to a dc level and superimposing a dc offset on-top of the data signal.

The V_H and V_L clamp levels, obtained using pre-

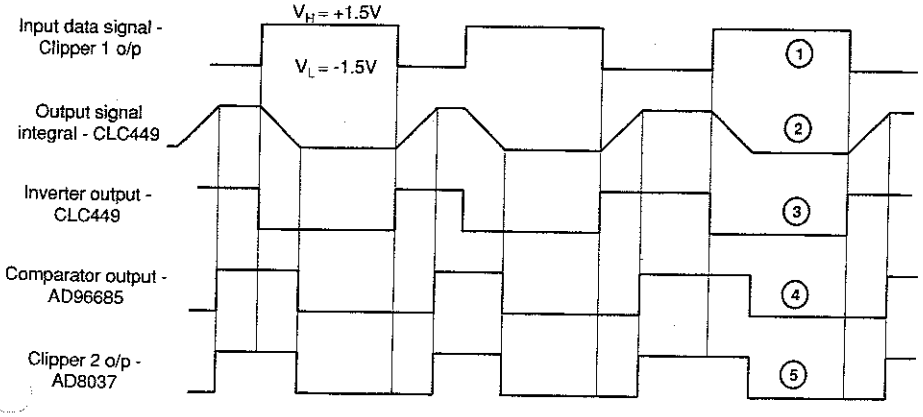

Fig. 2. Timing waveforms. Ramp output, waveform 2, is compared with the inverted version of the clamped date, 3, and when its amplitude reaches the inverted data input level, comparator output 4 changes state.

sion reference IC_8, were followed by a potential divider network and a quad operational amplifier, IC_9, used to buffer and invert the voltage taps from the potential divider.

The precision voltage reference circuit was tested for stability using a Keithley *195* precision digital multimeter. We found that each of the four output voltages varied by less than 1 part in 10,000 – i.e. 0.01% – when monitored separately over an eight hour period.

Adjustable-gain buffer IC_2 was set to provide a gain of 6 to compensate for the attenuation due to the three 100Ω output and 50Ω input matching resistor networks. Each of these introduced a signal attenuation of a third.

The *RC* time-constant of the active integrator, IC_3, is such that the output signal changed from one clamp level to the other in 24ns, whereby a positive or negative going linear ramp was produced when both the summing inputs change to

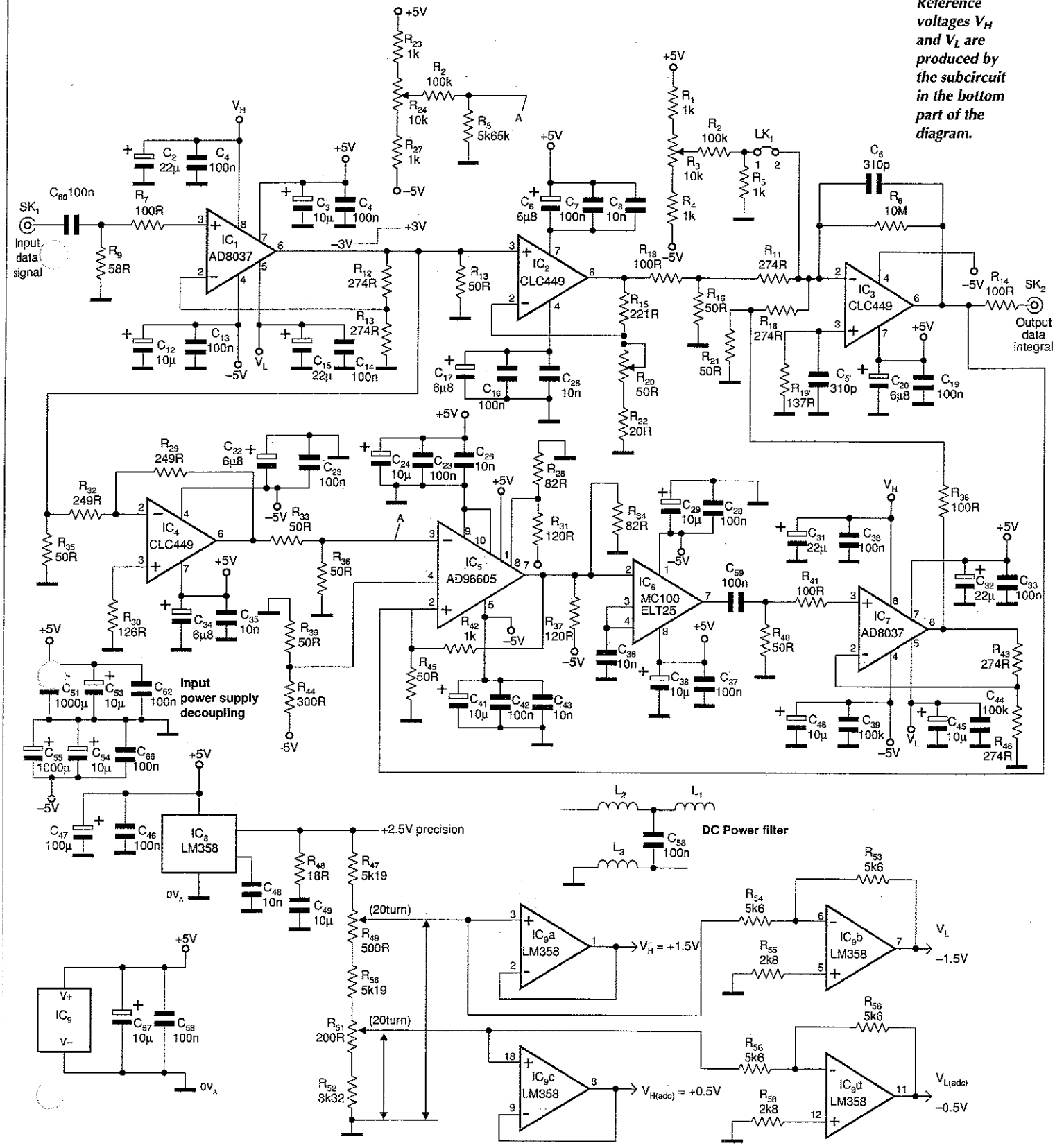

Fig. 3. Full circuit diagram for the precision integrator. Reference voltages V_H and V_L are produced by the subcircuit in the bottom part of the diagram.

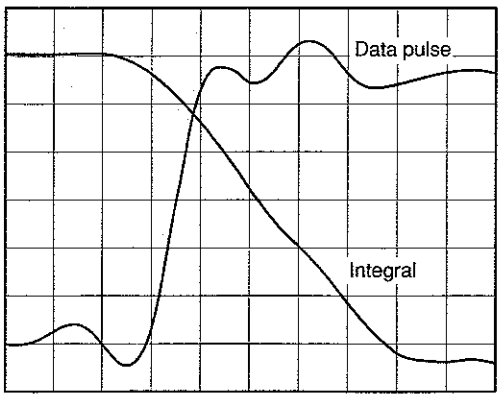

Fig. 4. Rising edge of data pulse with corresponding clamped integral at 1ns/div. The integral is 200mV/div while the data pulse is

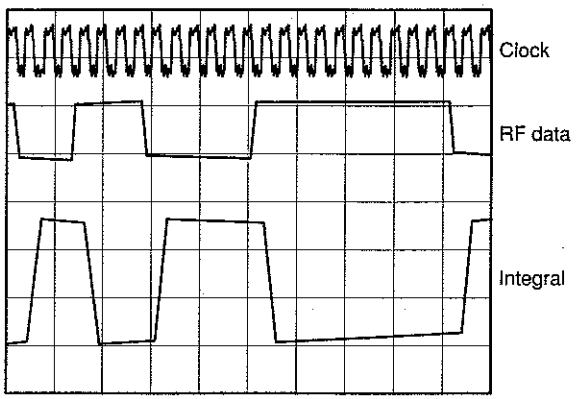

Fig. 5. Clock signal, input data signal and integrated-data signal at 100ns/div. Clock 5V/div, rf data 2V/div and integral 1V/div

a high or low state respectively, Fig. 2. It is most important to ensure that the summing resistors, R_{11} and R_{19}, are balanced.

Final circuit values were tuned for optimal performance, from which the following values were obtained: 310pF for C_5 and $C_{5'}$, 274Ω for $R_{11,19}$ and 137Ω for $R_{19'}$. The integration capacitors are silver-mica and the resistors were precision 0.1% tolerance metal film.

Resistor R_6 is included to limit the dc gain of the integrator. Some input offset voltage adjustment capability is provided via a network consisting of resistors $R_{1\text{-}5}$. The output from the active integrator is fed back to the positive input of comparator, IC_5. Resistors R_{42} and R_{45} were included in this path to introduce approximately 38mV of hysteresis. This prevents indeterminate conditions from occurring at the output of the comparator.

The negative input to the comparator is fed with an inverted version of the clamped data signal, obtained using IC_4, R_{29}, R_{32} and R_{33}. A dc offset adjustment is also provided at the input to the comparator via a network consisting of resistors $R_{23\text{-}27}$.

Output from comparator IC_5 is converted to ttl using IC_6, an *MC100ELT25*, whose output is again converted into a positive and negative swing around zero via C_{59}. This provides the appropriate levels for clamping. The signal is then also precisely clamped to ±1.5V using IC_7, which is configured in exactly the same way as IC_1.

Finally, the feedback loop is closed by summing output from IC_7 with the buffered data signal at IC_3's inverting input.

And how did it perform?

The operation of the circuit was evaluated using data signals, in the format described earlier. Output from the circuit was monitored using a Tektronix *TDS540A*, which is a 500MHz digitising oscilloscope capable of sampling at a rate of 1Gs/s.

Example test results are given in Figs 4 and 5. Figure 4 shows the rising edge of a data pulse and the corresponding integral after the delay through the system has been removed using a Dallas *DS1020* programmable eight-bit delay line, which has a resolution of 0.15ns.

You can see that the slope of the output signal is linear, making it possible to discern the necessary data at various points on the slope using a fast a-to-d converter. It should be pointed out here that an extra delay needs to be introduced during the calibration routine to ensure that the measurement points are taken over the linear region of the ramp, i.e. only using the range 1/4 to 3/4. Here, the slope can be characterised by the equation for a straight line, from which the timing jitter can easily be calculated.

Note that the full detail of this procedure is out of the scope of this article. I should also point out that although the bandwidth limit of the oscilloscope is being approached, Fig. 4 shows that it is still possible to resolve the ripple and overshoot of the data signal. If ripple was present on the integral, then it would be shown superimposed on top of the output slope. This gives us confidence that the slope is in fact truly linear and the waveform shown is not a manifestation of an oscilloscope bandwidth limitation.

You can also see that the output voltage levels change from one clamp level to the other in around 24ns, as required. Figure 5 shows the 27MHz data clock, together with two data pulses of width I_3 and I_{10}, and the corresponding output from the integrator.

The diagram shows that there is a slight voltage drift from the negative clamp level during the 'hold' time. This slight drift is non-effectual in the overall results from the system. Although it shifts the negative clamp level to a level somewhat closer to zero than the desired –1.5V, we would sample at between the 1/4 and 3/4 amplitude points on the slope.

During recent calibration and test measurements on the circuit, we found that we were able to completely cancel the non-constant 'hold' level by carefully adjusting the input offset voltage at the inverting input to the active integrator, via adjustment of potentiometer R_3. Also, the clamping levels may be changed by adjustment of the dc offset voltage at the inverting input to the comparator, which is controlled using potentiometer R24.

In summary

Our precision analogue integrator uses the fastest analogue integrated circuits currently available. We have shown that the feedback loop design effectively controls the precision clamping of the output levels. Recent measurements carried out on the circuit indicate that it is possible to achieve a repeatability of 0.1% on successive ramps.

We found it difficult to obtain long-term stability over a temperature range outside room temperature since this is determined by individual device voltage variation with temperature, which is outside our control. This variation is not detrimental to the overall operation of the system since the circuit will be calibrated prior to each measurement run to compensate for all device delays and circuit variations.

The calibration routine also ensures that the measurements are taken only on the truly linear region of the ramp.

I would like to thank Richard Amey and Dr Adam Hoare, of Aerosonic Ltd, for allowing me to carry out the work described in this paper. Thanks also to Jim Lusk, also of Aerosonic Ltd, for help in producing the circuit diagram and prototype pcbs. ■

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