BRIDGE RECTIFIERS REVISITED

OR

HIGH-EFFICIENCY AC-DC CONVERTER/VOLTAGE MULTIPLIER

From an idea by D. A. J. Harkema

This article discusses an extension of the well-known single-phase, full-wave bridge rectifier to provide a high-efficiency voltage multiplier. The extension is based on a circuit developed by Dip.Eng. Th. Gisper, a Swiss engineer, who described his design in a paper entitled *HF-DC-Converter-Schaltung in der passiven Telemetrie* (Eidgenössische Technische Hochschule—ETH—Zürich 26 February 1988)

A conventional bridge rectifier is shown in Fig. 1. When terminal a of the transformer is positive, diodes D_2 and D_3 conduct and current flows through load R_L. When terminal b becomes positive, on the alternate half cycles of the transformer voltage, D_4 and D_1 conduct and current flows in R_L in the same direction and at the same level as before. The voltage across the load is equal to the peak value of the voltage across the transformer secondary less the potential drops across the diodes.

There are various ways of increasing the output of the rectifier and some of these are shown in Fig. 2, Fig. 3 and Fig. 4: a single-ended, a balanced and a bridge voltage doubler respectively. The circuit of Fig. 3 is used when a balanced d.c. output (with respect to earth) is required.

In Fig. 2, when a is positive, D_1 conducts and capacitor C_1 charges to the peak value of the a.c. input voltage. On the reverse half-cycle, D_2 conducts and C_2 also charges to the peak value of the input voltage. The charge on C_1 is retained, since D_1 is reverse-biased. Therefore, both capacitors charge to the peak value of the input voltage, so that the d.c. output voltage is equal to twice the peak input voltage. This is only true, however, when no load is connected across the output terminals.

With a load connected across the output, current is supplied to it by the discharge of the capacitors. On alternate half cycles, the capacitors are recharged. This means that the output voltage is a direct voltage with an a.c. ripple superimposed on it. This ripple is minimized by making the capacitors as large as is practically possible, taking into account the current drain and the frequency of the a.c. input voltage.

The circuit in Fig. 4 is a better type of voltage doubler. It has two important advantages over that of Fig. 3. The first is that the frequency at which the capacitors are charged is twice as high, so that the ripple voltage is reduced. The second is that the load on the transformer remains the same even when the loads on the two d.c. outputs are different.

The Gisper development is basically a combination of the bridge rectifier of Fig.1 and the voltage doubler of Fig. 2 as shown in Fig. 5a, or a synthesis of the circuits of Fig. 3 and Fig. 4, as shown in Fig. 5b.

Briefly, the circuit of Fig. 5a works as follows. It will be assumed that the a.c. input is sinusoidal and has a peak value of 20 V. During the first quarter of a period, capacitors C_2 and C_3 are charged via diodes D_4 and D_6 to a potential of +20 V. When the a.c. input decreases, D_4 is re-

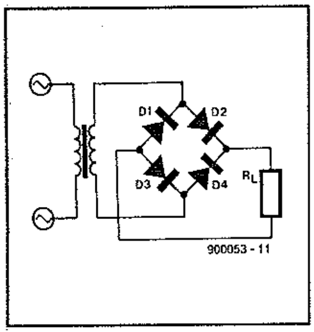

Fig. 1. Conventional bridge rectifier.

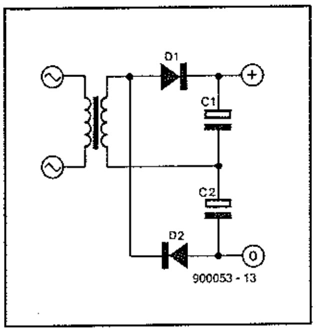

Fig. 2. Single-ended voltage doubler.

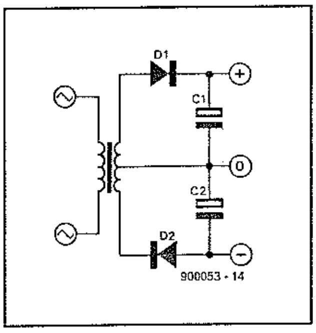

Fig. 3. Balanced voltage doubler.

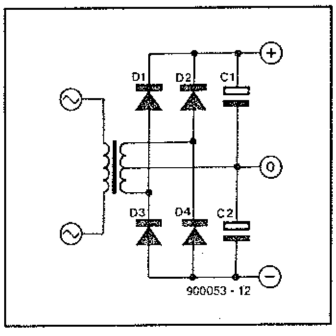

Fig. 4. Bridge voltage doubler.

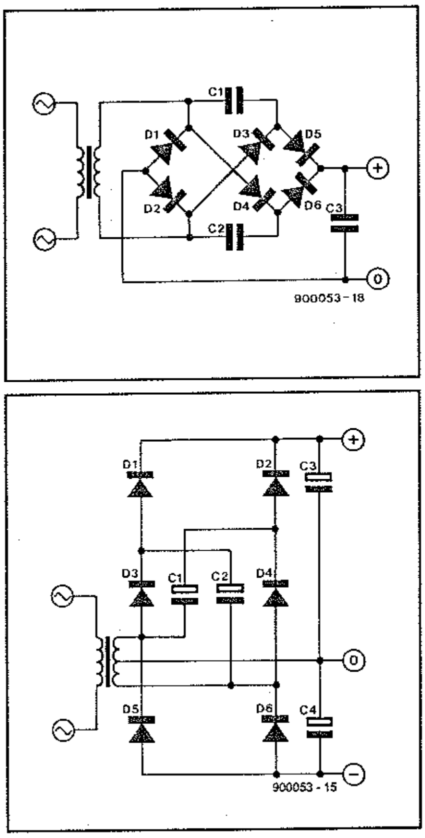

Fig. 5. The Gisper design is a combination of the bridge rectifier of Fig. 1 and the voltage doubler of Fig. 2 as shown in (a) or a synthesis of the rectifier in Fig. 3 and the voltage doubler of Fig. 4 as shown in (b).

verse biased and the voltages across C_2 and C_3 are maintained at +20 V.

When the a.c. input passes through zero, D_3 conducts and C_1 is charged to +20 V. At the same time, C_2 discharges via D_6 and C_3 via D_1 to a value of +10 V. The voltage at the junction D_1-C_1 changes from +20 V to –20 V. This causes C_3 to be charged to +30 V. The potential across D_1+D_2 is then –20 V.

As soon as the a.c. input rises, D_1 is reverse biased. The voltage across capacitors C_1 and C_2 remains +10 V and +20 V respectively. This causes the potential at junction C_1-D_3-D_5 to rise and reach a value of +30 V when the input reaches +10V. When the input rises to +20 V, the

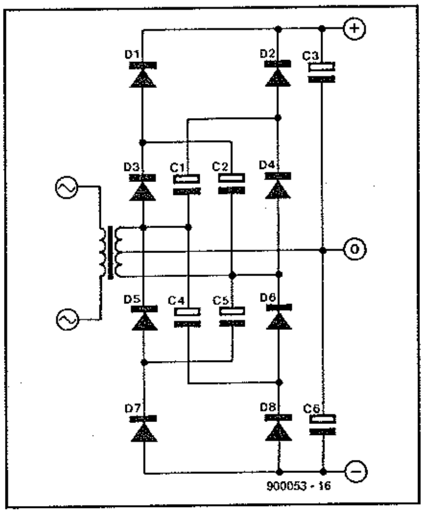

Fig. 6. The Gisper bridge may be extended as shown. The addition of each pair of diodes and capacitors raises the d.c. output voltage by a value equal to that across one half of the basic bridge rectifier.

potential across C_3 rises to +34 V.

At the moment the input exceeds +10 V, the voltage across C_2 rises from +10 V to +20 V, while that across C_1 decreases to +16 V.

When the input decreases, D_5 is reverse biased. The voltage across C_2 remains +20 V and that across C_1, +16 V. As soon as the a.c. input becomes more negative than –16 V, C_1 is charged via D3 to +20 V. At the same time, the potential across C_2-D_6-C_3-D_1 attains a value of –20 V, that across C_2 drops to +17 V, and that across C_3 rises to +37 V.

When the a.c. input increases again, the process described repeats itself. Within a few cycles, the voltage across C3 has risen to +40 V and that across C_2 to +20 V.

It appears that the Gisper bridge can be extended as shown in Fig. 6 and Fig. 7. The addition of each pair of diodes and capacitors raises the output voltage by a value equal to that across one half of the bridge rectifier. It is also possible when further extending the circuit of Fig. 6 to tap voltages at various points of the diode network as shown by the dotted lines in Fig. 7. ■

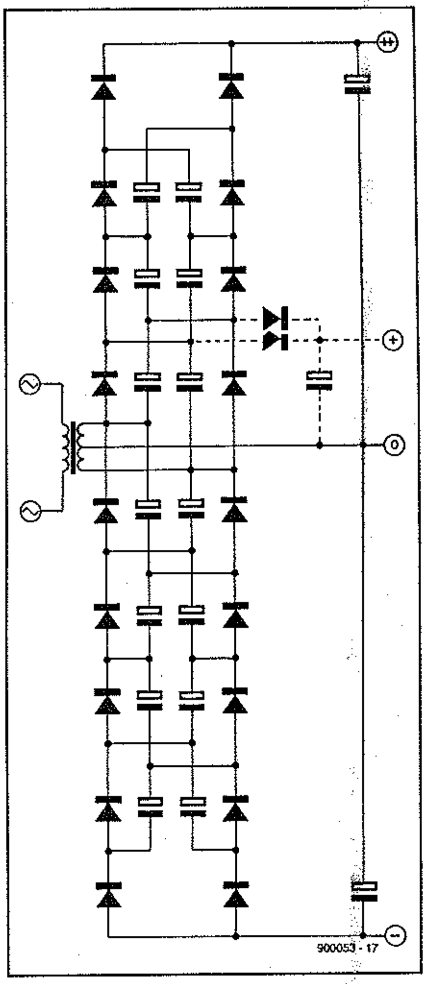

Fig. 7. When further extending the circuit of Fig. 6, it becomes possible to take off voltage at various points in the circuit as shown here by the dashed lines.

Sources:

Th. Gisper: *HF-DC-Converter-Schaltungen in der passiven Telemetrie*: Semesterarbeit an der Professur für elektrotechnische Entwickelungen und Konstruktionen, ETH Zürich, 26 February 1988.

Elektronica, 17 November 1989, "Spanningsverdubbelaar met hoog rendement".

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