BIG surprises... ...small packages

At one end of the surface-mount spectrum, complex digital ICs are becoming so densely pinned that they make prototyping almost impossible. At the other, it is now easy to obtain one logic function or op-amp in a single, minute sm package. While reducing product size, these tiny devices can simplify implementation, improve performance, and even open up new application areas, as Ian Hickman demonstrates.

The surface-mount revolution has been under way for years now, with most products using surface-mount passives. Fixed resistors are migrating from the 1208 size, with dimensions of 0.12 by 0.08in, to 0805, 0604 or even 0402.

Trimmer resistors, with overall dimensions of less than 4mm square are supplied by several manufacturers, including Bourns and Citec. Capacitors are available in a similar range of sizes to fixed resistors, though the larger values such as tantalum electrolytics tend to still be in 1208 or larger format, for obvious reasons.

Trimmer capacitors are available with a footprint of less than 4mm square, from various manufacturers, including Murata. Surface-mount inductors are available in the various formats. Ingenious surface-mount carriers accommodate ferrite toroid cored inductors where higher values of current-carrying capacity or of inductance are necessary – such as in switchmode power supplies – and where the extra height can be accommodated.

But surface-mount passives have been around so long that there is not much new to say about them. So this article concentrates on active devices, and mainly on integrated circuits, which is where the action currently is.

Recent trends

More recently, there has been renewed interest in really tiny devices with eight, five or even just three pins. This format has long been favoured by rf engineers, for uhf and microwave transistors, the consequent reduction in overall size and lead lengths contributing to minimal package parasitics.

Now, the advantages of really tiny devices, which are many, are becoming available also to analogue and digital designers, and this article looks at some of these devices. **Table 1** lists typical examples, giving the package designation – which varies somewhat from manufacturer to manufacturer – the number of pins, a typical example of a device in that package, and its manufacturer, and the maximum overall size of the 'footprint' or board area occupied by a device in that package style. This again varies slightly from manufacturer to manufacturer.

With devices in such small packages, getting the heat away can be a problem. With many of these ICs, though, the difficulty is alleviated due to two aspects. Firstly, many devices such as op-amps, comparators and digital ICs now work from a single supply of 3V or even lower, as against the 5V, ±5V or even ±15V required by earlier generations. Secondly, with improved design techniques, high-speed wide frequency range devices can now be designed to use less current than formerly.

Nevertheless, thermal considerations still loom large in many cases, when applying these tiny devices. This is discussed further in the following sections, which deal with various classes of small outline devices.

Discrete active devices

With discretes such as diodes, in many cases maximum dissipation is a pressing consideration, and package styles and sizes reflect this. Thus the *UDZ* series zeners from Rohm, in the SOD-323 package, **Fig. 1a)**, are rated at 200mW. But *RLZ* series devices, also from Rohm, in the slightly larger LL34 package, Fig. **1b)**, dissipate 500mW, while the *PTZ* series in the even larger PSM package, Fig. **1c)**, is rated at 1W.

With active devices also, special packages are used to cope with the device dissipation. International Rectifier's *IRFD11x* series mosfets for example are mounted in a four pin 0.3in DIL package, **Fig 2a)**. Pins 3 and 4 are commoned and provide not only the drain connection, but also conduct heat to through-hole pads on the pcb, which help dissipate the heat.

These surface-mount devices have a P_{drain} rating of 1.2W. This is actually 20% more than the rating of the *VN10KM*, which is housed in a TO237 package, see Fig. **2b)**. The TO237 is like a TO92 package, but it has a metal tab, connected to the drain, projecting from the top.

The SOT89 is an even smaller package, Fig. **2c)**, measuring just 2.5 by 4mm, excluding leadouts. Nevertheless, the Rohm *BCX53* is rated at 500mW, or 1W when mounted on a suitable ceramic pcb. The wider collector lead, on the opposite side of the package from the base and emitter leads, bends back under the body of the device, providing a large heat tranfser area.

The SOT223 package, not shown, provides a power dissipation of up to about 1.5W at 25°C. The TO252 'D-pak' shown in Fig. **2d)**, housing for example an *IFRF024* 60V, 15A mosfet with 60A pulsed I_d rating, does even better. The device dissipates watts, provided

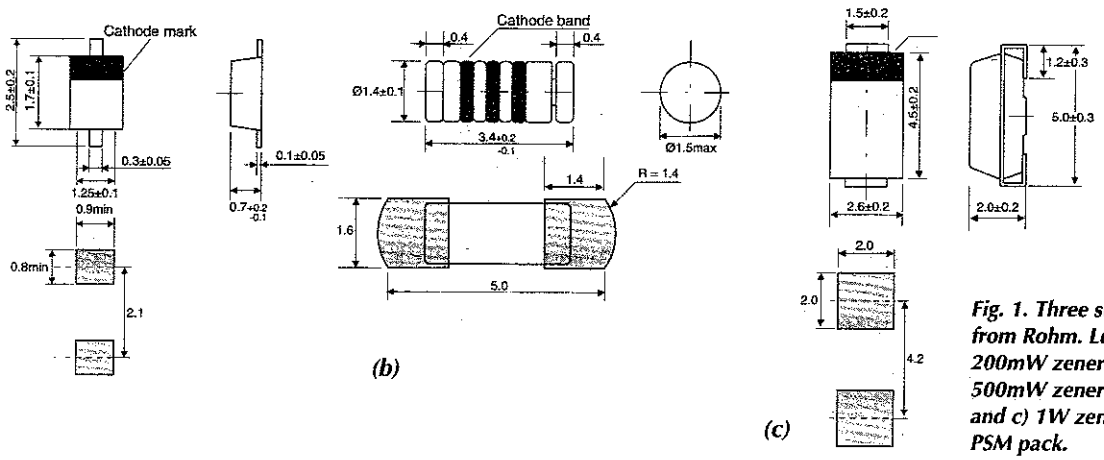


Fig. 1. Three surface-mount diodes from Rohm. Left to right are a) 200mW zener in SOD-23 package, b) 500mW zener in the larger LL34 pack and c) 1W zener in the even larger PSM pack.

that you can keep its case temperature down to 25°C.

For small signal amplifiers, size is less important and transistors are available in packages smaller than SOT23 (SMT3), **Fig. 3a)**. The UMT3 (Ultramold, SOT323) package of Figure **3b)** has a footprint of 2.2mm by 2.2mm overall, including leads, while the EMT3, Fig. **3c)** occupies just under 1.8 by 1.8mm overall, these being the maximum dimensions.

With such very small devices, traditional laboratory prototyping becomes very difficult, not to say tedious.

Analogue ICs

With digital ICs, the tend is to higher and higher levels of functional integration, with an inevitable accompanying inflation in the number of pins per package. In the analogue world however, general purpose functions, such as op-amp, comparator, buffer and voltage reference tend to dominate. The result is that while digital ICs tend to get bigger – or at least not much smaller, due to all those pins – analogue functions are appearing in smaller and smaller packages.

The exception is d-to-a and a-to-d converters with parallel data buses. But these ICs tend to bridge the analogue/digital divide anyway. And even here, devices in tiny eight-pin packages are readily available, thanks to the economy in pin numbers afforded by using serial data input/output schemes rather than bus structures.

While single transistors can be mounted in packages smaller than SOT-23, this is more problematical for the larger silicon die of ICs. So for the most part, the three pin version of SOT-23 is the smallest package used for ICs. An example is the *AD1580* 1.2V micropower precision shunt voltage reference, from Analog Devices.

To the user, the *1580* appears simply as a 1.2V zener diode. But the dynamic output impedance (ac slope resistance) at 1mA is typically just 0.4Ω, resulting in a change in output voltage, over 50µA to 1mA and over –65 to +125°C, of only 500µV typical. Being a two terminal device, pin 3 has no conection, or may be connected to the negative supply.

A good example of an op-amp in a small package – also available in an eight-pin DIP – is the *LMC7111*, from National Semiconductor, **Fig. 4**. The leadout arrangement of the five-pin SOT23-5 version is shown in Fig. **4a)**: note the actual size drawing alongside!

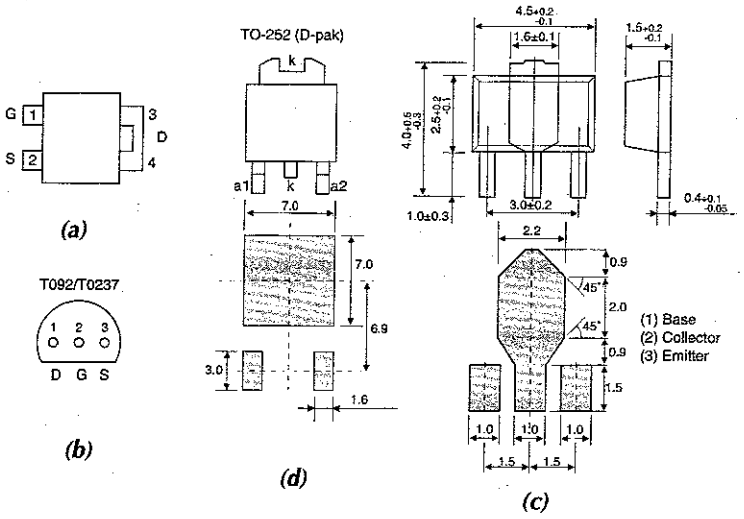
The device is a c-mos op-amp with rail-to-rail input and output, operating from a supply voltage V_s of 2.7V upwards to an absolute maximum of 11V). With a gain/bandwidth product, or gbw, of 40kHz with a 2.7V supply, it draws a supply current I_s of around 50µA. Its bipolar stablemate, the *LMC7101*, offers a 0.6MHz gbw and 0.7V/µs slew rate in exchange for an I_s of around 800µA, also at 2.7V.

Table 1. Some representative devices in small packages, from various manufacturers. 'Small outline' is abreviated to SO.

Style	Leads	Example	Function	Manufacturer	Footprint max
SOD-323	2	1SS356	Diode, band-switch	Rohm	1.35x2.7mm
SOT23-3*	3	LM4040AIM3-5.0	Voltage ref. 5V 0.1%	Nat. Semi.	3.0x3.05mm
SOT23-5**	5	AD8531ART	Op-amp, 5V, 0.25A o/p	Analog Devices	3.0x3.1mm
SO-8	8	MAX840	–2V reg. GaAs fet Bias Generator	Maxim	5.03x6.29mm
SO-14	14	LT1491CS	Quad op-amp, 2-44V supply	Linear Tech.	6.20x8.74mm

*'TinyPak', TM. Also known as TO-236-AB
**JEDEC TO-xxxxx outline definition now due

Fig. 2a). Four pin 0.2in DIP package often used for fets and other smallpower devices. At b) is the TO237 pack is like a TO93, but with a small metal tab extending from the top, c) the SOT89 pack can typically dissipate 0.5-1W and d) TO252 package dissipates watts – provided you can keep the case temperature below 25°C!



Need more speed?

Where something a little faster is needed, then in the same package, and from the same manufacturer comes the *LM7131* high-speed bipolar op-amp. This has a gbw of 70MHz, and a slew rate of 100V/µs – even when driving a capacitive load of 20pF. Total harmonic distortion at 4MHz is typically only 0.1% when driving a 150Ω load with a 3V V_s. Even with this level of performance, I_s is only 8mA.

Where blindingly fast speed is necessary, the *LM7121* voltage feedback op-amp, in the same package with the same pinout, has a 1300V/µs slew rate, for an I_s of just over 5mA

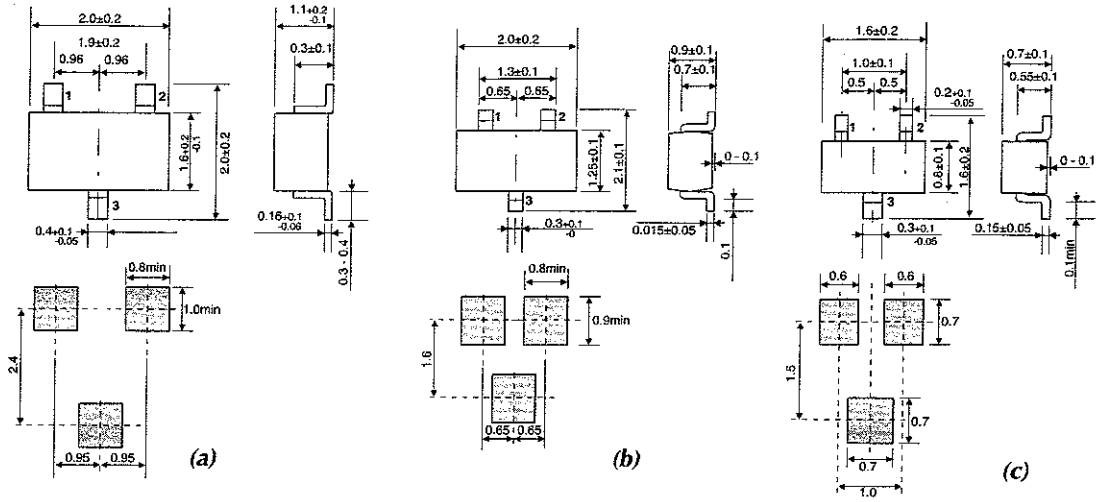


Fig. 3 . Three small transistor outlines: the tiny SOT23-3 a) dwarfs the SOT323 at b), which in turn dwarfs the miniscule EMT3 at c).

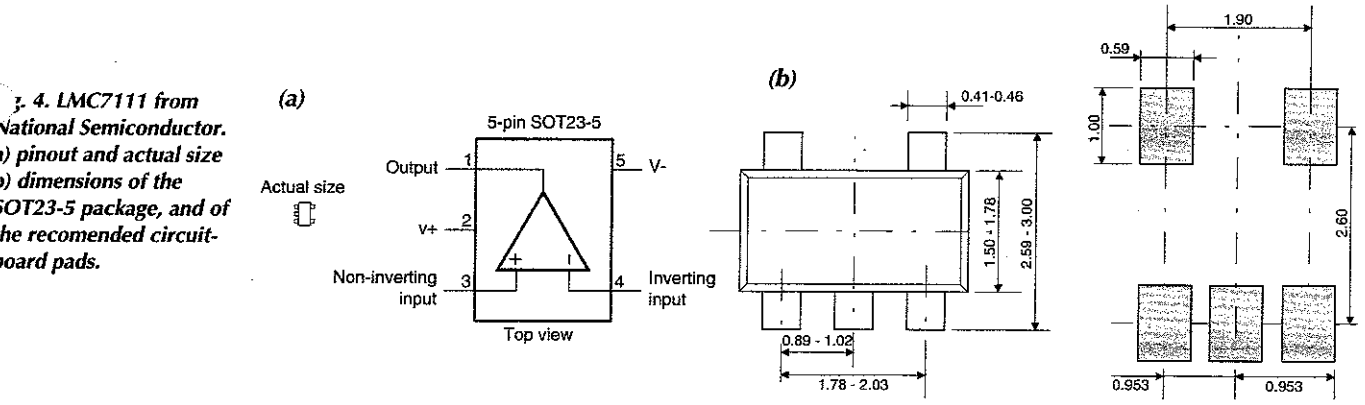


Fig. 4. LMC7111 from National Semiconductor. a) pinout and actual size b) dimensions of the SOT23-5 package, and of the recomended circuit-board pads.

typical. But note that this is the performance with dual supplies of +15 and −15V. The device works on a single V_s of down to 5V, but the performance is then more modest.

Unusually for an op-amp, this device is stable with literally any level of load capacitance, maximum peaking, up to 15dB, occuring with around 10nF. Other stablemates in the same SOT23 package and with the same pinouts, are the *LMC7211* and *LMC7221* rail-to-rail output comparators, with active and open drain outputs respectively.

Current feedback op-amps are known for their excellent ac characteristics. The *OPA658* is a wideband low power current feedback opamp from Burr-Brown, available in the SOT23-5 pin package. With a unity gain stable bandwidth of 900MHz and a 1700V/µs slew rate, it has a wide range of applications including high resolution video and signal processing, where its 0.1dB gain flatness to 135MHz is exceptional.

Where a circuit requires two op-amps, two separate devices in, say, SOT23-5 packages may be used. This provides the ultimate in layout flexibility and it may even take up less space than a dual. But the dual op-amp will usually be cheaper than two singles.

Figure 5 shows the *AD8532* dual rail-to-rail input and output c-mos op-amp from Analog Devices. Featuring an output drive capability of a quarter of an amp and a 3MHz gain:bandwidth product with a V_s of 5V, it operates from a single supply in the range 2.7 to 6V.

Figures **5a)** and **b)** compare the footprint in the TSSOP, or thin shrink small outline package, and the SO-8 package. Width over the pins is similar, but the TSSOP's pin spacing of 0.65mm, against twice this for the SO-8, results in a package length not much more than half that of the SO-8. For applications where more space is available, the device also comes in the old-fashioned 8 pin DIP package.

Figure **5c)** shows the op-amp's internal circuitry in simplified form. As common in devices with a rail-to-rail input, whether bipolar or fet, complementary input pairs in parallel are used. Likewise, for rail-to-rail outputs, common drain (collector) stages are dropped in favour of common source (emitter) stages.

Figure **5d)** shows the clean large signal pulse response, even at a Vs of just 2.7V. The device is just one of the family of *AD8531/2/4* single/dual/quad opamps, available in a wide variety of package styles.

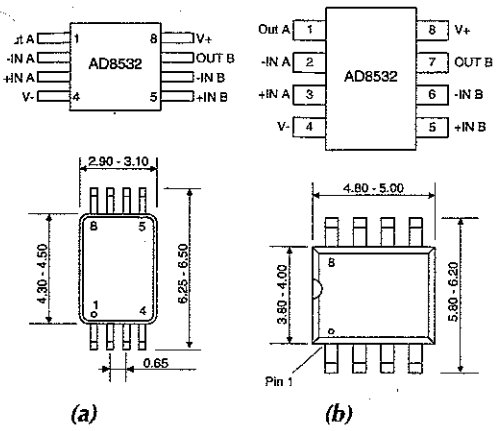
Another dual op-amp, this time with the exceptional V_s range of 2.7V to 36V, is the *OPA2237*, from Burr-Brown. With its maximum offset voltage of 750µV and its 1.5MHz bandwidth, it is targeted at battery powered instruments, PCMCIA cards, medical instruments etc. It is available in SO-8, and also in MSOP-8, or micro small outline package, which is just half the size of the SO-8 package.

Traditional packaging options

For years, ICs came in just two widths, and a variety of lengths, all with pins on 0.1in centres. Thus 8, 14 and 16 pin dual-in-line DIL devices – whether side brazed ceramic types to military specifications, or commercial plastic moulded DIPs – came with a width between the two rows of pins of 0.3in.

For ICs with 24, 28, 40 or 68 pins however, 0.6in was the order of the day. Even so, there were exceptions, such as 0.3in 'skinny' 24-pin devices. But then, with the appearance of more and more complex ICs, more and more i/o pins were necessary. To accommodate these, square devices with pins on all four sides appeared, such as chip-carriers – both leadless and leaded, J lead devices and plastic quad flatpacks (PQFP) with various pin centre spacings, often only 0.025in or less, and up to 200 pins or more.

To minimise package size, ICs were packaged in 'pin-grid array' packaging, with several parallel rows of pins on the underside of each edge, and again up to 200 or more pins. Yet other formats are SIL/SIP (single in line/plastic) packages for memory chips and surface-mount audio frequency power amplifiers. Audio power amplifiers also appear in through-hole mounting SIPs, with alternate pins bent down at different lengths, to mount in two rows of staggered holes.



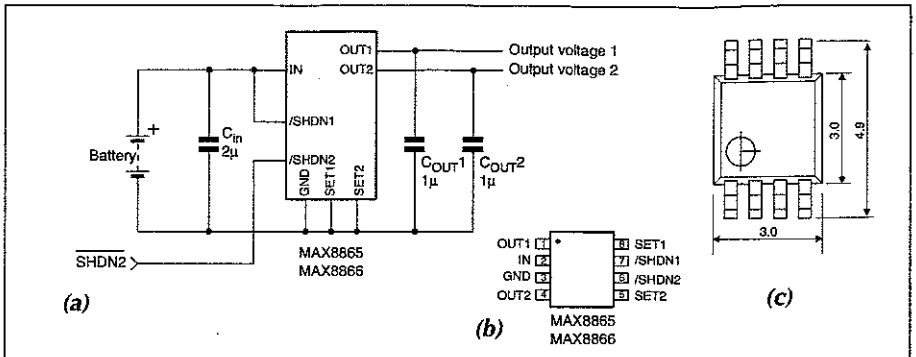
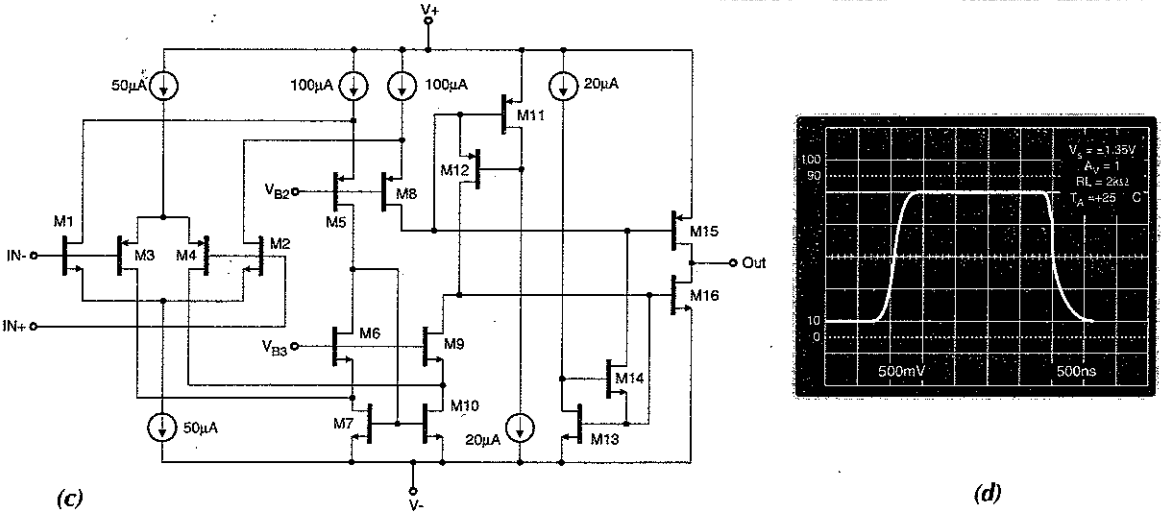


Fig. 6. MAX8865x dual low-dropout regulator a) from Maxim comes in the proprietary muMAX package, with pinout as at b). At 3mm, package length c) is similar to TSSOP, but the width across pins is 1.5mm less, which could lead to its more widespread adoption by other manufacturers.

Fig. 5. AD8532 dual op-amp from Analog Devices is available in TSSOP a), SO-8 b) or 8-pin DIP. The parallelled complementary input stages and common source output stages provide rail-to-rail operation at both ends c). The 2V peak to peak response, operating on ±1.35V rails, is shown in d).



Other analogue circuits

Figure 6 shows the Maxim *MAX8865x* dual low drop-out regulator, where suffix *x* is *T*, *S* or *R*, indicating preset output voltages of 3.15, 2.84 or 2.80V respectively. Each output is capable of supplying up to 100mA, with its own individual shutdown input.

Figure **6a)** shows the device conected to supply output 1 continuously, and output 2 only when the /SHDN2 pin is high. If the SET1 or SET2 pin is connected not to ground, but to a voltage divider connected across the corresponding output, the circuit produces whatever stabilised output voltage results in the SET pin being at 1.25V. This assumes of course, that the input voltage,which must be in the range 2.5 to 5.5V, is adequate.

Internal circuitry for each output senses whether the SET pin is at a voltage below or above 60mV, and selects an internal, or the external voltage divider respectively. The pin allocation is as in Fig. **6b)**, while the package dimmensions are given in **c)**. This package is proprietary to Maxim. It is the same length as an eight-pin TSSOP, but with a narrower body, making the width over the pins rather smaller. The *MAX8866* is similar, but includes an auto-discharge function, which discharges an output to ground whenever it is deselected.

Figure 7 shows two other Maxim devices. At **a)**, are shown the *MAX4051* and *MAX4052*, these being single normally-open and normally-closed analogue switches respectively. Mounted in SOT23-5 packages, they are used where a single switch function is needed, providing it in much less space than would be occupied by a quad analogue switch pack.

At **7c)** is shown the *MAX864* dual-output charge pump. This provides outputs of +2Vin and $-2V_{in}$ nominal, for any input V_{in} in the range +1.75 to +6.0V. Two pins, FC0 and FC1, are connected to ground or V_{in} as required, offering a choice of four different internal switching frequencies in the range 7 to 185kHz, assuming that the /SHDN pin is high. The *MAX864* is packaged in a QSOP outline, Fig. **7b)**.

Figure 8 shows a 12-bit d-to-a converter, the *LTC1405*, from Linear Technology. It accepts 12-bit parallel input data and outputs up to 4.095V or 2.048V (pin strappable selection), from a 4.5 to 5.5V supply. The *LTC1450L* provides a 12-bit resolution output of up to 2.5V or 1.22V, from a 2.7 to 5.5V supply.

Figure **8a)** shows the internal workings of the chip, which is available mounted in a 24 lead SSOP package, **b)**, or in a 28 pin DIP. Figure **8c)** shows the companion *LTC1458/1458L*, which is a quad 12-bit d-to-

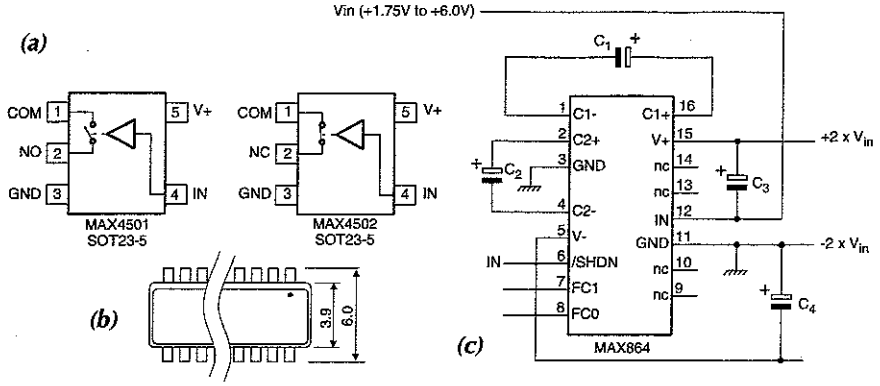


Fig. 7a). Single normally-open or normally-closed analogue switches save space compared to leaving a quarter of a quad pack unused. b) is the MAX861 package and c) is the pin-out and application circuit.

a converter. It is shoe-horned into a 28 pin small-outline package, or a 28-pin SSOP, by using a serial data input scheme, rather than the parallel data input of the *LTC1405/L*.

Figure 9 shows another d-to-a converter, this time one which accepts 16 or 18 bit data. It is designed for use in compact-disk systems, MPEG audio, MIDI applications, etc. The *PCM1717E* from Burr-Brown incorporates an eight-times oversampling digital filter, multi-level delta-sigma d-to-a converter and analogue low-pass in each of its stereo output channels. Its selectable functions include soft mute, digital de-emphasis and 256 step digital atttenuation. Using a serial data input, it is supplied in a 20-pin SSOP package, a shorter version of that shown in Fig. 8b).

Digital alternatives

Traditional small and medium-scale integration logic circuits – originally supplied in 0.3in width packages with up to 16 (later, 18, 22 or more) pins – have long ago migrated to the SO and even smaller packages.

Large-scale integration devices with up to 64 or 68 pins came in 0.6in wide packs, but then migrated to a variety of package types, including leaded and leadless chip carriers, J-lead packs, pin-grid arrays etc. The latest development in packaging is ball-pin arrays.

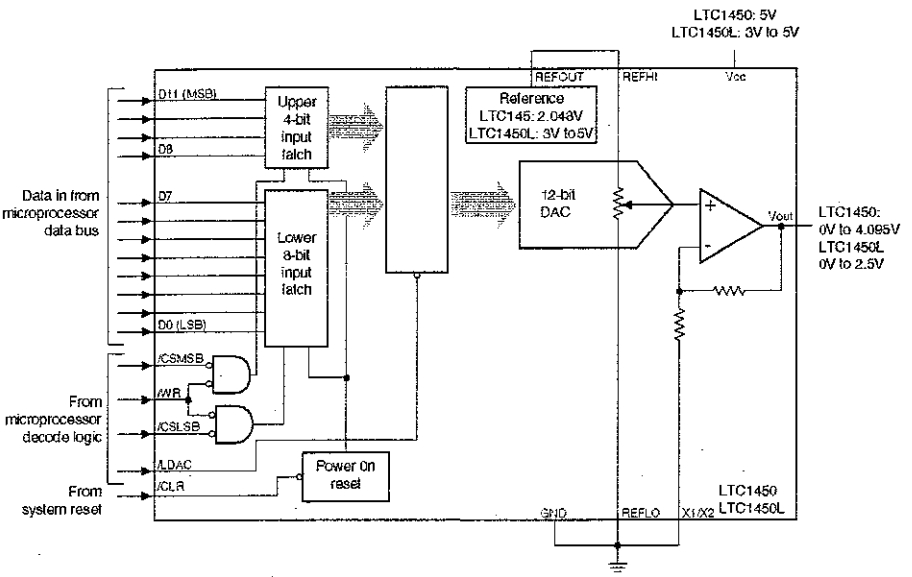
But processors, dsp chips and the like tend to require so many leadouts that they hardly come under the heading of tiny devices, even though truly small considering the number of pins. This is illustrated in **Fig. 10**, which shows packages with a modest 44 pins, **c)** and **d)**; 52 pins, **b)**; and 240 pins, **a)**. This latter package even comes in a version with 304 pins.

In addition to processors, dsp chips etc, package types with a large number of pins are also used for custom- and semi-custom logic devices, and programmable arrays of various types. These enable all the logic functions associated with a product to be swept up into a single device, reducing the size and cost of products which are produced in huge quantities.

But this approach is not without its drawbacks, often leading to practical difficulties at the layout stage. For example, on a densely packed board, the odd logic function such as an inverter, AND gate or whatever, may be required at the opposite end of the board from that at which the huge do-it-all logic package is situated. This forces the designer either to accept long digital signal runs right across the board, or to include a quad small-scale integration package, of which only a quarter is used, or to seek some other solution.

Discrete logic

Such a solution is now at hand, right at the other extreme from multi-pin packs, or even 14-pin small-scale integration quad-gate packs. For example, a simple resistor/transistor logic, or rtl, inverter can be implemented with a 'digital transistor' as shown in **Fig. 11 a)**, using a surface-mount resistor as collector load.



(a) These digital transistors, from Rohm, are available in the tiny three pin packages shown in Fig. 3, with a variety of values for R_1 and R_2. For example, type *DTC144ExA* is an npn transistor where R_1=R_2=47kΩ. Suffix *x* is a code indicating which of the three

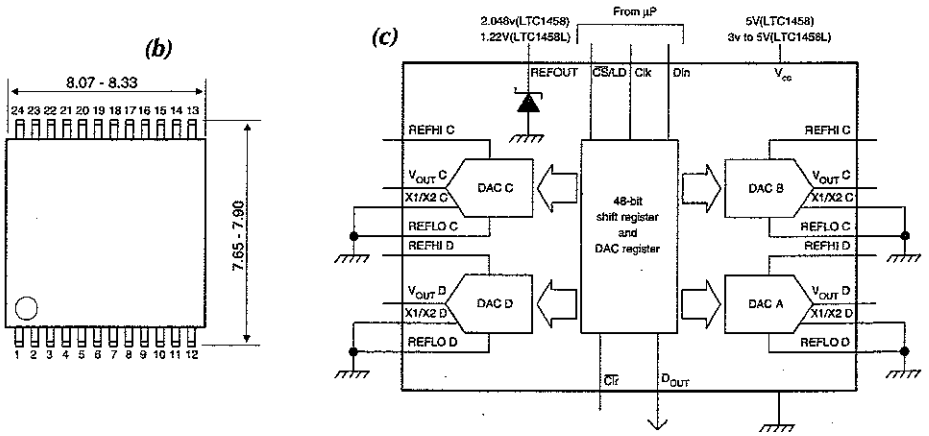


Fig. 8. LTC1405, a), from Linear Technology is a 12-bit d-to-a converter with parallel data input. This reqires a 24-pin package, b), but the SO small-outline pack is still much smaller than the corresponding DIP.
c) shows a block diagram of the internal workings of the LTC1458, from the same manufacturer. This quad d-to-a converter comes in an SO pack, or the even smaller SSOP. Both have only 28 pins, achieved by using a 48-bit serial data input stream.

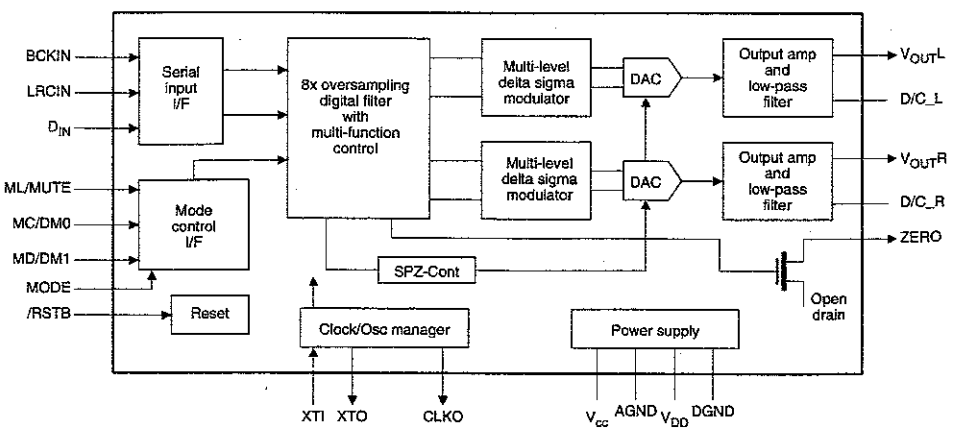


Fig. 9. Burr-Brown's PCM1717E d-to-a converter accepts 16 or 18 bit serial data, and provides L and R stereo output channels. With numerous facilities, aimed at cd systems, MPEG audio, MIDI applications etc.

These digital transistors, from Rohm, are available in the tiny three pin packages shown in Fig. 3, with a variety of values for R_1 and R_2. For example, type *DTC144ExA* is an npn transistor where R_1=R_2=47kΩ. Suffix *x* is a code indicating which of the three packages of Fig. 3 applies.

Adding another such transistor connected to the same collector load provides the NOR function, while connecting them as in Fig. **11b)** gives the inverse EXOR or exclusive NOR function. With three separate components, this provides just about the most flexible layout possibilities that could be devised.

However, a single component solution is also possible. Nearly all the functions which are available in quad small-scale integration packs are also available as singles in the SOT23-5 pack. One example has already been illustrated in Fig. 7a).

Suppose for example that an EXOR gate were required, this is readily available in c-mos as the *NC7S86M5*, see Fig. 11c) and d), from National Semiconductor, along with AND, NAND, OR, NOR gates etc. The device quoted operates from supplies of 2V to 6V, sinks or sources 2mA and has a typical propagation delay T_{pd} of 4.5ns.

As well as the large packages of Fig. 10, special purpose digital ICs are available in the smaller packs discussed here. A good example is the *REG5608*, which is an 18-line SCSI (small computer systems interface) active terminator chip from Burr-Brown, **Fig. 12.** On-chip resistors and voltage regulator provide the prescribed SCSI bus termination, while adding only 2pF per line – important for SCSI FAST-20 operation.

All SCSI terminations can be disconnected from the bus with a single control line. The chip output lines then remain in a high impedance state with or without power applied. This is important for 'hot socket' equipment plugging. The device is available in both 28-pin SOIC and fine pitch SSOP packages.

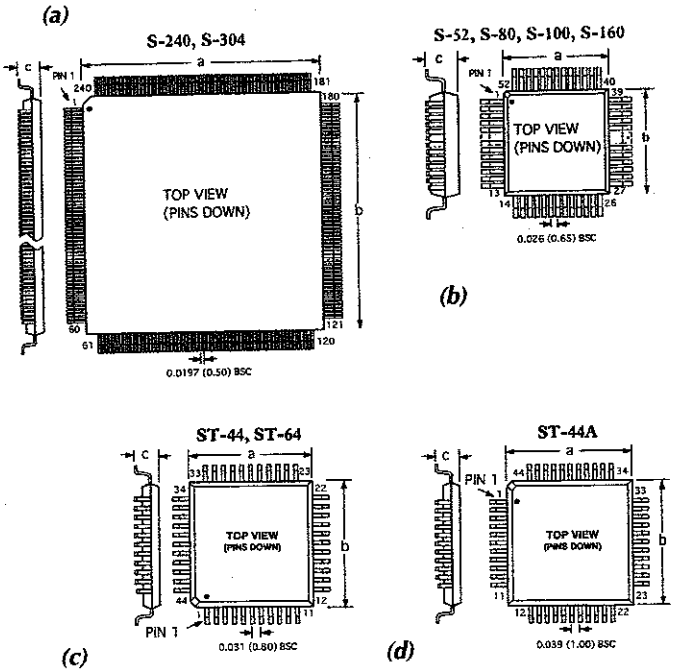


Fig. 10. Digital ICs come in packs with up to 300 pins – or more. a) shows the 240-pin PQFP (plastic quad flatpackage) S-240. The slightly wider pin spacing of PQFP packs with up to 160 pins, b), is more manageable. There are traps for the unwary! The two 44-pin TQFP (thin quad flat package) packs in c) and d) look very similar, but the pin spacing is different.

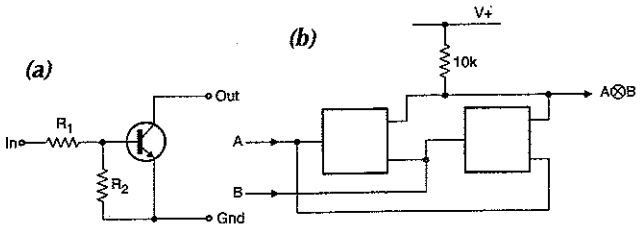


Fig. 11. Digital transistors, a), from Rohm, are available in SOT 23 packs, Fig. 3, with a variety of values for R_1 and R_2. Two such transistors connected as in b) give the inverse EXOR or exclusive NOR function. A single component solution is also possible, being readily available in c-mos as the NC7S86M5, c) and d), from National Semiconductor

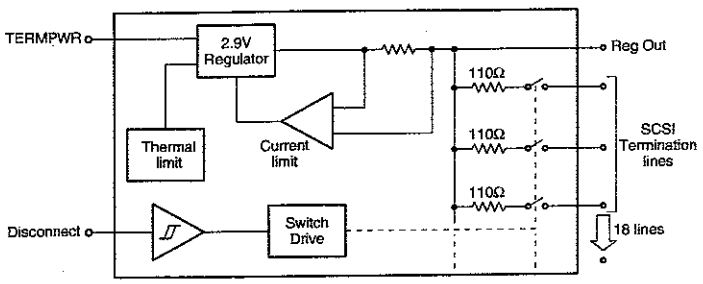


Fig. 12. REG5608 is an 18-line SCSI (small computer systems interface) active terminator chip from Burr-Brown. On-chip resistors and voltage regulator provide the prescribed SCSI bus termination. A single control line open circuits all the terminations, important for 'hot-socket' equipment plugging. The device is available in both 28-pin SOIC and fine pitch SSOP packages.

Technical considerations

When using the very small types of components discussed here, a somewhat different approach is called for, compared with ICs in DIPs and other easily handled parts.

The practical difficulties of conventional breadboarding have already been mentioned. With these very small parts, designers often go straight to pcb design from simulation to avoid the difficult job of prototyping. In any case, if the circuit involves one or more of the fine pin-pitch multi-pin devices, some of which are illustrated in Fig. 10, then a circuit-board layout will be required at the outset anyway.

Simulation is eased by the availability of Spice models for many of these devices; even if not, an op-amp model using just the input capacitance, first and second breakpoints and the output resistance may prove adequate.

It is useful to add a few strategically placed pads or plated-through holes to provide test-points for use in evaluation and debugging. This is safer than trying to probe pins which are spaced a millimeter or less apart.

Manufacturers face various problems producing very small parts. One concerns packaging, where the package dimensions may not be much larger than the basic silicon chip itself. For example, the *LT1078/9* and *LT1178/9* family of single-supply op-amps in standard DIP format from Lineear Technology are justly popular. They exhibit very low supply currents of 55μA and 21μA per op-amp respectively. But the same devices in the surface mount SO outline exhibit worse maximum input offset voltage V_{OS}, and offset voltage drift. This is because the plastic surface mount packages, in cooling, exert stress on the top and sides of the die, causing changes in the offset voltage.

continued on page 404

source as shown below,

$$P_{10}(V)=(V-10)^2/2+V^2/10+(20-V)^2/4+20((V-20)/4)$$

Minimizing this function gives a node voltage V of 8.82V as can be seen by the plot of the power function, **Fig. 5**.

However, the actual node voltage is 11.765V[1]. This result can be obtained by introducing a 'resistance' defined by

$$R_{20V}=4V/(V-20)$$

Now the power equation is,

$$P(V)=(V-10)^2/2+V^2/10+(20-V)^2/4+400/R_{20V}$$

Minimizing this equation where R_{20V} is treated as a constant leads to the correct value of 11.765V as verified by the node voltage method.

As demonstrated by the above circuits, the authors' approach of minimizing the power function does not always work since the concept of a stationary turning point does not exist in circuits with constraints other than resistive constraints. Therefore, the only way to handle these circuits is to replace the non-resistive elements with a 'resistance' defined by the quotient of its voltage and current. By treating this resistance as constant, just as the real resistances are constant, partial differentiation will lead to the correct gradient and ultimately the correct node voltages. ■

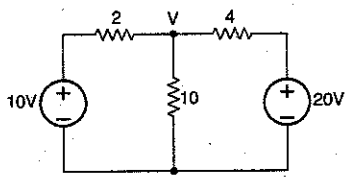


Fig. 4. Circuit containing more than one independent source.

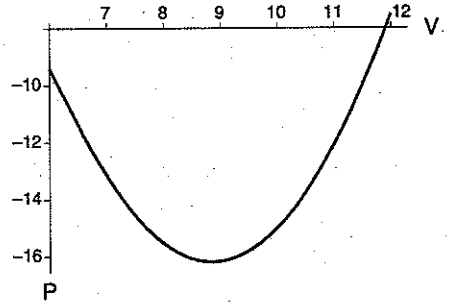


Fig. 5. Power function plot.

Standard analysis techniques

Standard approach to solving the transient response of the first circuit presented:

$$i(t)=i_\infty+(i_0-i_\infty)e^{\frac{-t}{\tau}}$$

where $i_\infty=2.5A$

and $\tau=\frac{0.0016}{20}$sec.

$i(t)=2.5-2.5e^{-12500t}$amps

Node voltage approach to solving the second circuit presented:

$V_1/4+(V_1-V_2)/5+(V_1-50)/2=0$

$V_2/20+(V_2-V_1)/5-1.7(50-V_1)=0$

solving this simultaneous system of equations leads to V_1=43.26V and V_2=80.46V

Node voltage approach to the third circuit:

$V/10+(V-10)/2+(V-20)/4=0$

V=11.765V.

BIG Surprises... small packages

contiued from page 374

In response to this problem, Linear Technology has introduced the *LT2078/9, 2178/9* range. These new devices use a thin, approx 50µm thick jelly-like coating, applied before encapsulation, to reduce stress on the top of the die. This results in significantly better V_{os} and V_{os} drift.

Manufacturers also face problems with the marking of these very small parts. The capacitance value is marked on AVC ceramic chip capacitors, for example, in neat clear print. But the print is so tiny it can only be read with the aid of a powerfull eyeglass.

Integrated-circuit designations tend to be quite long, so manufacturers are often obliged to use abbreviated codes to designate a part. For example, the SOT23-5 packaged *NC7S86M5* exclusive OR gate of Fig. 11 is marked simply '*7S86*' on the top, while the similarly packaged *LMC7101BIM5X* op-amp, also from National Semiconductor is marked *A00B*.

Standard sizes?

Figure 10 illustrates another point that you should be aware of when using these devices – watch out for the mechanical dimensions. While the two 44-pin devices illustrated in Figs 10c) and d) look very similar, the pin pitch on the ST44 in c) is 0.8mm, while that on the ST44A in d) is 1mm.

Pin connections are another possible trap. The connections for a single op-amp in the SOT23-5 package shown in Fig. 4a) are the commonest variety, used by a number of manufacturers. But some SOT23-5 op-amps use pin 1 and 3 as inputs, with pin 2 ground, and the output on pin 4.

With todays's densely packed boards, multilayer circuit-board construction is the order of the day. Usually, the inner planes carry power while the signals run on the top and bottom planes. Interconection between top and bottom planes, often used for mainly horizontal and mainly vertical runs respectively, is by plated-through hole vias. Conections to or between inner layers may be made using 'blind' vias.

Unfortunately, the minimum pitch of conventional plated-through holes is greater than the pitch of the pins on many packages. So adjacent plated-through holes have to be stagered. This takes up more board space, negating some of the advantages of the very small packages.

A more recent development – namely microvias – provides a solution, but at a cost. These vias are so small that they can be located within the land area of each pin's pad, permitting much closer spacing of ICs.

Real benefits

Although more difficult to apply than their larger counterparts, these very small devices benefit the designer in many ways.

For example, two single op-amps in SOT23-5 packages occupy about half the board space of a dual op-amp in an SO-8 pack. Additionally, even more space saving may accrue, due to the greater flexibility afforded by two separate packages. Each can be place exactly where needed, minimizing circuit-board trace lengths.

The problem of needing the odd gate, right across the other side of the board from a bespoke masked logic chip or ASIC containing all the other logic, has already been mentioned. Individual gates and buffers such as that in Fig. 11 clearly supply the answer. But they have another use, no less important.

Single logic elements can be used to buffer the output of an ASIC, found to be over loaded at board evaluation stage. They can even be used to implement a minor last minute logic change, without the cost and delay penalty of having to redesign the ASIC – provided that at the layout stage, the designer took the precaution of leaving the odd spare scrap of board area here and there.

With all their advantages, tiny ICs, both analogue and digital, are destined to play in increasingly important role in today's electronic world, where time-to-market is all important. ■