Driving on the high side

Ian Hegglun

demonstrates how high-voltage high-side switching, ac switching and half-bridge switching can all be done reasonably fast using low-cost logic gates and small-signal diodes.

Half-bridge mosfet drivers usually use two n-channel mosfets because n-mosfets offer lower on resistance. But this complicates the gate drive for the high side mosfet. Integrated circuits for driving half bridges are now available. They reduce the component count but for some applications, they are either too expensive or do not allow control of the dead time.

A relatively simple discrete high side drive can be made using a voltage doubler, **Fig. 1**[1]. Here, a high-frequency oscillator drives a voltage multiplier which charges the mosfet's gate capacitance. When the oscillator signal is gated off the gate resistor R_g discharges the mosfet gate capacitance. This is simple, inexpensive but relatively slow. A number of methods described here can improve the speed and usefulness of this method.

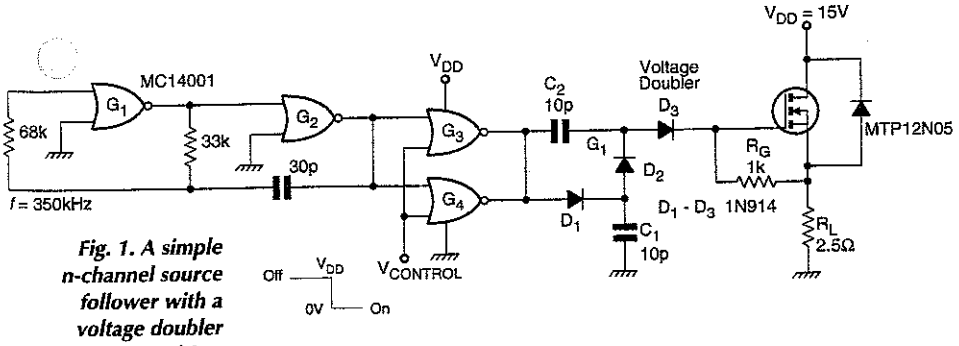


Fig. 1. A simple n-channel source follower with a voltage doubler drive.

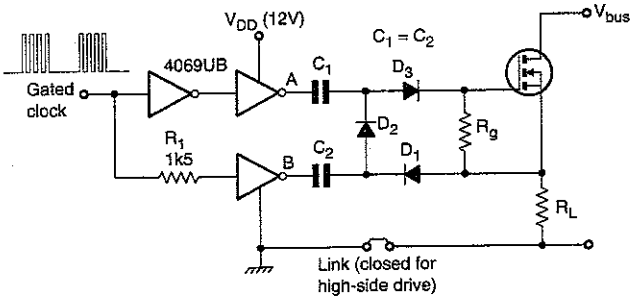


Fig. 2. The improved voltage doubler allows the mosfet to be turned on with the link open.

Improving on the doubler

Figure 2[2] uses the improved voltage doubler which allows the mosfet source voltage to rise to a higher voltage than in Fig. 1. Reference 2 includes a mains mosfet driver using this doubler technique. Analysis of the high side version (link closed) can be broken into three stages. First, with the link open and no voltage for supplying the load, then with supply voltage added and finally with the link closed.

With the link open and no load supply, start with no charge on the coupling capacitors $C_{1,2}$. When the inverters are powered up one output will be high and the other low. If output A is high then current will flow through C_1 and D_3 then through the mosfet's gate-source capacitance and back through D_1 and C_2. This causes C_1 and C_2 to be charged to nearly half V_{DD} while placing some charge on the mosfet's gate-source capacitance.

During the next phase, current flows through C_2, D_2 and C_1, which re-polarises the capacitors to around half V_{DD}. The next phase is a repeat of the first, except that C_1 and C_2 now have more than zero volts across them which allows the gate voltage to rise further.

Eventually, the gate-source voltage reaches a limit. If R_g is removed, the limit is $2V_{DD}$ less two diode voltage drops. When running c-mos gates on 12V the doubler output can reach 22V off load.

When R_g is added the final voltage is reduced because R_g forms a voltage divider with the output resistance of the doubler R_{out}. With a 12V supply the value of R_g should not be less than R_{out} because the gate voltage is pulled down to half of 22V when R_g=R_{out} or 11V which is usually sufficient for standard mosfets.

When R_g equals R_{out}, gate charging time constant T=RC can be found. The total capacitance is C_{iss}+2C_1 and a net resistance of R_g//R_{out} when turning on the mosfet. For turn off there is C_{iss}+2C_1 but only R_g for discharging. This makes turn off typically twice as long as the charging time constant if R_g equals R_{out}.

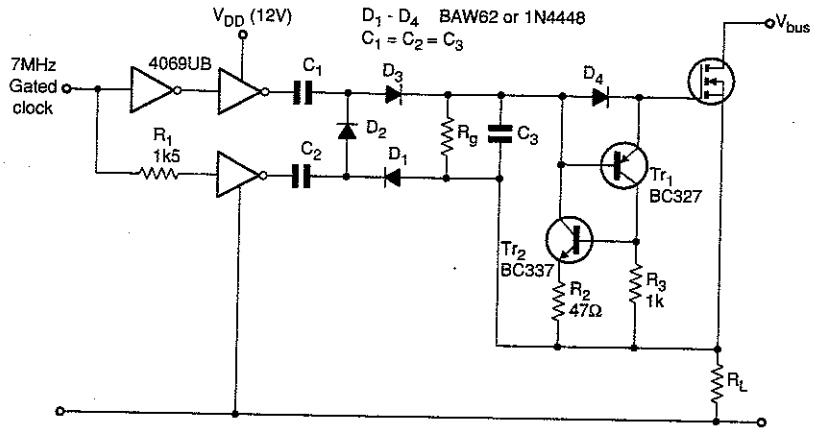


Fig. 3. Adding a regenerative clamp reduces turn off time to 1µs and allows higher frequency operation.

Next, with the link still open and a floating supply to drive the load the rise and fall times for the gate voltage increases due to the Miller effect. It is a rapidly changing drain-source voltage V_{ds} that causes current to flow through the mosfet's drain-gate capacitance C_{dg} which opposes gate current used to switch the mosfet. This current typically doubles the turn on and turn off transition times and the effect can be observed on the gate voltage waveform as a plateau region, similar to those shown in most mosfet data sheets. More on this is given in the panel entitled 'Mosfet input capacitance'.

For high-side switching, the link is closed. The circuit continues to operate as before except that C_1 and C_2 must be charged ultimately to the load voltage. This requires current flow through the link. When the mosfet turns on, this is not a problem but when switching a high voltage, the turn-off time is increased considerably. When switching high voltages such as 300V from the mains, the turn-off time is 10 to 20 times longer than the turn-on time. This restricts the switching frequency to only low switching rates.

The speed difference can be explained. When the mosfet begins to turn on, there is a path for current from the source through D_1 and C_2 to rapidly charge C_1 and C_2. This is a form of boot strapping where the mosfet is acting with near unity voltage gain with an input capacitance much less than C_{iss}. But when the drive to the mosfet is stopped Rg must discharge C_1 and C_2 starting from the load voltage down to zero.

Current through R_g holds up the gate-source voltage above V_t until C_1 and C_2 have discharged sufficiently. The effect is observed as an extended plateau when turning off.

Achieving faster turn off...

To speed up the high side driver a turn-off clamp was developed. The standard single-transistor p-n-p clamp, as used in PIV isolators[3], did not reduce the turn off time of the high side drive although it did assist turn off when the link was open.

A regenerative scr type circuit, **Fig. 3**, is needed to speed up the clamp the gate voltage when the gate begins to be discharged by R_g. When drive to the doubler is stopped, the mosfet gate discharges through Tr_1 which turns on the second transistor Tr_2, triggering the latch. This discharges the mosfet gate capacitance rapidly as well as the coupling capacitors through the link and load. Resistor R_2 limits the discharge current through C_1 and C_2 and drivers.

Capacitor C_3 prevents ripple from the doubler output triggering the scr. A full-wave doubler is helpful here to reduce the ripple and allow C_3 to be a small value ($0.1C_1$) which increases the rise time by up to 25% but requires two extra capacitors – all capacitors are halved – plus three diodes.

With these extra components, the turn off time can be reduced to much less than the turn on time. Fall time can be 1µs with 300V even with large gate capacitance. Turn on time is now the limiting factor.

...and faster turn on

Mosfet turn on time in any mosfet drive is limited by the magnitude of current that can be delivered to the mosfet to charge the gate-source capacitance. In a multiplier drive this current is limited by the coupling capacitors reactance and the driver's source resistance.

There is little point increasing C_1 more than half the mosfet's gate capacitance because more driver energy is wasted charging C_1 and C_2 than is delivered to the mosfet. This places a practical limit on C_1 and C_2 in the range of 1nF to 4nF (the value of C_{iss} for the mosfet used).

Raising the clock frequency to the highest possible frequency for full output swing is the best way maximise turn on time and minimise the coupling capacitance.

From tests the effective capacitive reactance seen at the output was found to be about seven times the capacitive reactance for a sinewave. Reactances of C_1 and C_2 appear in series and

Mosfet input capacitance

Current is required to charge the input capacitance of a mosfet to turn it on. Input capacitance is mostly gate-to-source metallisation and gate to channel capacitance plus some parallel gate to drain capacitance. Capacitance C_{iss} is the common source input capacitance and is the sum of C_{gs} and C_{dg} (on data sheets C_{gd} appears as C_{rss}.

Both C_{gs} and C_{dg} are voltage dependent and vary considerably with V_{ds} when V_{gs} is a few volts below or above V_{ds}, or V_{dg} is approximately zero. Calculation of gate voltage rise time based on data sheet C_{iss} value at V_{ds}=25V will give a value that is 200 to 400% too fast.

A better method to find the gate voltage rise time is from the effective C_{iss} value derived from the gate charge graph. The effective input capacitance is calculated from $C=Q/V$ where V is the gate voltage rise required to turn the mosfet on and Q is the charge required to reach that voltage. The rise time can be estimated from 2.5 RC time constants – assuming it is supplied by the same V used above – where R is the driver source resistance in parallel with the gate discharge resistor, if used.

The plateau region is caused by the Miller effect while V_{ds} is changing[6]. This means rise and fall times can be found from $Q=ixt$, where Q is the charge required to move through the plateau region and i is drive current at this point where i is constant here because V_{gs} is constant. Hence $i=(V_s-V_{pl})/R_s$. Voltage V_{pl} is typically 3-4V for non-logic mosfets – a volt or two above V_{TH} – or can be found from the V_{gs} versus I_D plot from the load current.

Simple rules of thumb can be used for rough estimates. The effective input capacitance is around three times the data sheet C_{iss} value, at V_{ds}=25V, when charging of the gate to 10V. Rise and fall times for the load voltage will be around half the gate voltage rise time found from the C_{iss} estimate and gate driver source resistance. can be measured on a capacitance meter by shorting the drain to source together. This give C_{iss} at V_{ds}=0 and the effective C_{iss} value is around 1.5 times higher for 10V gate driving.

There are undoubtedly exceptions so use the gate charge method when ever possible.

ewise the driver resistances but these must be referred to the output like a transformer with a 2:1 step up ratio and is seen as $8R_{on}$ at the output. Hence we have $R_{out}=14X_c+8R_{on}$, where X_c is $^1/_{2\pi fC_1}$.

Equating $14X_c=8R_{on}$ gives,

$$C_1 < \frac{1}{3.6 f_{max} R_{on}}$$

and $R_g>16R_{on}$. **Table 1** shows measured values R_{on}, f_{max} for various drivers and calculated values for C_{1max} and R_{gmax} for use in Fig. 3.

Rise-time values are calculated using $t_r=2.5(R_g/2)(3C_1+C_{iss})$ where C_{iss} is 1.5nF – the effective value for the *BUK453-100A*. While the 74xx04 inverters offer low output resistance they are not suited to driving standard mosfets because of their 6V maximum supply. They are still useful for driving logic level mosfets. A tripler can be used if a 12V supply is not available, but loading on the drivers is doubled and the rise time increased.

The 4041B is a quad buffer with complementary outputs and internal equalisation delay. It offers the best performance but at higher cost. Farnell's list its price at about four times that of the 4049B. Complementary outputs for standard inverters can be obtained by the method shown in Fig. 3 and explained in the 'Speed trial' panel.

Table 2 shows measured rise and fall times for Fig. 3 driving a *BUK453-100A* mosfet (10A, 100V) with 22V into a 50Ω load. Rise time is not affected significantly when driving a 5Ω load or higher voltages although the fall times do increase with higher voltage. The fast discharge circuit allows the fall time can be kept small at higher voltages.

Note t_r for the gate voltage in this table is not the usual 10% to 90% measurement, but rather the time for the gate voltage to reach 10V from 0V. With R_g increased, the final voltage is closer to 15V.

The fast discharge circuit allows R_g to be higher than the minimum in Table 1 without affecting the discharge time. Faster gate voltage rise times recorded in Table 2 can be partly attributed to the higher R_g values. Note that if R_g is too large, the gate voltage may exceed the maximum allowable so a 15V zener diode should be placed across R_g for protection.

I was intending to apply this in switched capacitor converters[4]. Because electrolytic capacitors are used in these converters for charge pumping, the best operating frequency is around 30kHz. The drivers described here are more than adequate for this. The 4041B with all four buffers in parallel can drive a 4nF mosfet for 0.5µs transition times provided the coupling capacitance is also increased.

Table 1. Test results for c-mos inverters operating at 12V predict reasonably gate voltage rise times in the range of 1.5-10µs or 1-2 orders of magnitude faster than PIV relays.

	Measured			Calculated		
	V_{DDmax}	R_{on} (Ω)	f_{max} (MHz)	C_{1max} (pF)	R_{gmax} (Ω)	t_{rmin} (µs)
4069UB	15	270	7	150	4k3	10.5
4049UB	15	150	11	170	2k4	6.0
4049B	15	150	12	150	2k4	5.9
4041B	15	60	10	460	960	3.5
74HCU04	6	50	16	350	800	2.5
74HC04	6	50	17	330	800	2.5
74VHCU04	6	50	20	280	800	2.3
74AC04	6	20	18	770	320	1.5

Table 2. Measured rise and fall times for various c-mos drivers using the values shown when driving a BUK453-100A as in Fig.3. Only one pair of inverters are used as drivers in all cases.

	Test values			Gate voltage		Load voltage	
	C_1 (pF)	R_g (Ω)	f (MHz)	t_r (µs)	t_f (µs)	t_r (µs)	t_f (µs)
4069UB	220	10k	7	6	1	2	0.5
4069UB	150	10k	7.5	6	0.5	1.5	0.2
4049B	220	4k7	12	2.5	0.5	1	0.3
4041B	470	4k7	10	1.5	1	0.5	0.5

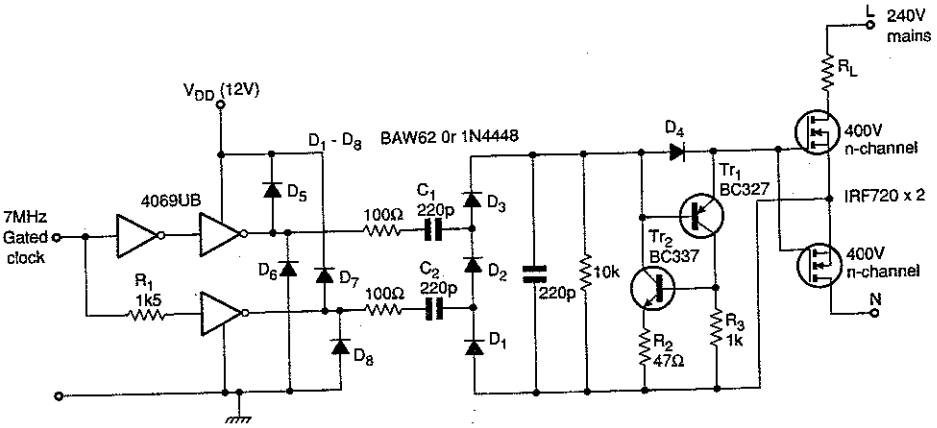


Fig. 4. With two mosfets ac can be controlled from ground potential but protection is needed to prevent high current spikes coupled through $C_{1,2}$ from damaging the c-mos drivers.

Solid state ac switch

Figure 4 shows a circuit that was used to chop 240V mains at several kilohertz. The driver should be ground referenced for safety but can be connected to any other potential if required.

Protection diodes and resistors are needed on the inverter outputs to divert current spikes caused by abrupt common mode voltage changes. The values shown protect the 4069 against mains spikes. To demonstrate this the driver common can be directly connected to phase while running – of course in this test the driver supply must be floating.

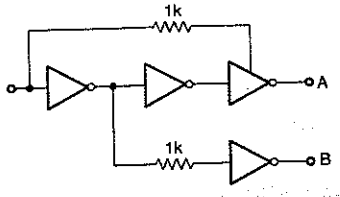
The 4049 or 4041 provides an extra margin of reliability for mains operation, although for harsh, noisy environments it would be wiser to use a high common mode dv/dt optocoupler instead of this method.

This ac switch was intended for use in a flying capacitor circuit[5], to allow the output of a bridge rectifier to be connected back to ground for safety, **Fig. 5**. This overcomes the need for a transformer. It operates as follows. Mosfets A_1 and A_2 charge the flying capacitor while B_1

Speed trials

The propagation oscillator is a type of phase-shift oscillator which uses the phase shift of three stages to set the operating frequency. Overall phase shift required is 180° or 60° for each stage if they are identical.

The 4069UB, 4041B and 4049B give close to full output swing with a 1kΩ resistor between one stage to lower the operating frequency slightly for full output swing. The *74XX04* types require an additional additional 1kΩ resistor between stages plus a 10pF capacitor to ground on the inputs supplied by the resistors. Complementary outputs can be obtained by adding a fourth inverter with a 1kΩ delay equalisation resistor as shown.



Propagation oscillator for c-mos inverters, as used in the speed trials.

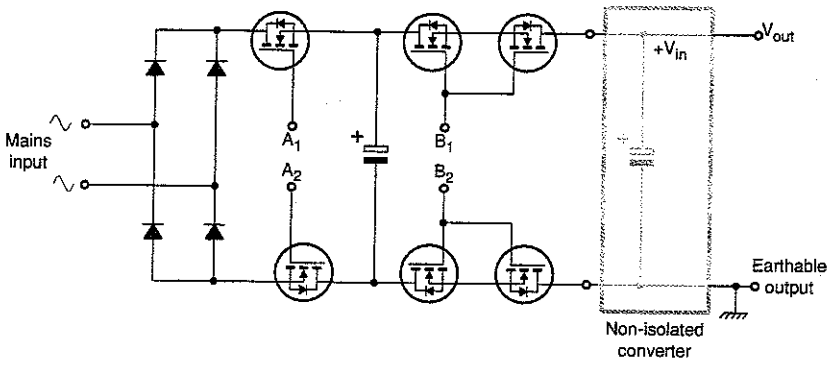


Fig. 5. The flying capacitor technique allows the normally floating output of a bridge rectifier to be connected to earth without damaging the circuit.

and B_2 are off. Fets A_1 and A_2 turn off before B_1 and B_2 turn on. When B_1 and B_2 turn on charge is transferred to the converter. Non-overlapping switching is essential when the output is connected to earth.

Note that this method does not allow the output to 'float' like a transformer because the mosfets must withstand mains voltage plus any common mode difference plus a safety margin.

A crowbar circuit and earth leakage protection should be used to protect against excessive common-mode voltage, which can destroy the mosfets and place mains on the output. With 500V mosfets and 230V mains, only 100V common mode difference is allowable.

Higher margins are offered by igbts at reasonable cost, namely 500V margin with 1kV devices, but tail losses limits the frequency to under 10kHz.

All four mosfets require high side drivers although *A* and *B* mosfets can share the same driving gates and control circuit. Regulations in some countries place a limit on the amount of coupling capacitance between line and earth of 0.005µF which allows four drivers each with up to 470pF coupling capacitors. This amounts to a reasonably safe current of 300µA from 230V.

Half-bridge drive

I have tested the half-bridge circuit of **Fig. 6**, and found that it can operate at 100kHz using the humble 4069. Three outputs are paralleled to drive a two diode charge pump, $D_{5,6}$, plus a doubler. The charge pump provides twice the current of the doubler in the plateau region around 3V and accelerates gate charging and reduces the turn on time. Once above this region the doubler takes the voltage to 10V.

The propagation oscillator, see the 'Speed trial' panel, is a feature that allows the drivers to run at the maximum frequency to suit the particular device used – 7MHz for the 4069 used here. Dead time is adjustable by delaying the turn on signal to each mosfet. The ability to reduce dead time improves the form factor and efficiency when operating at high frequencies. I have found the inability to adjust dead time on the *IR2151* to be a limitation when operating above 50kHz.

In summary, a wide range of applications can make use of this method of driving mosfets where the source voltage is different from the driving circuit common. High voltage high side switching, ac switching and half bridge switching can all be done reasonably fast using low cost logic gates and small signal diodes. No high-voltage transistors or opto-isolators are required.

My thanks to National Semiconductor for supplying complementary samples of the *74VHCU04*. ■

References

1. Motorola, Power Mosfet Data, Q1/88, 1988, p1-6-21.
2. SGS-Thompson, Power Supply Application Manual, July 1985, AN275, p277-280.
3. Moore, D. W., 'Using Photovoltaic relays in multiplexers', *Electronics & Wireless World*, July 89, pp. 725-8. (or International Rectifier note GBAN-PVI-1).
4. Hegglun, I., 'Stepping out', *Electronics World*, October 1996, pp. 759-806.
5. 'Novel power supply', *Electronics & Wireless World*, September 1988, p. 885.
6. International Rectifier, AN947, 'Understanding HEXFET® Switching Performance'.

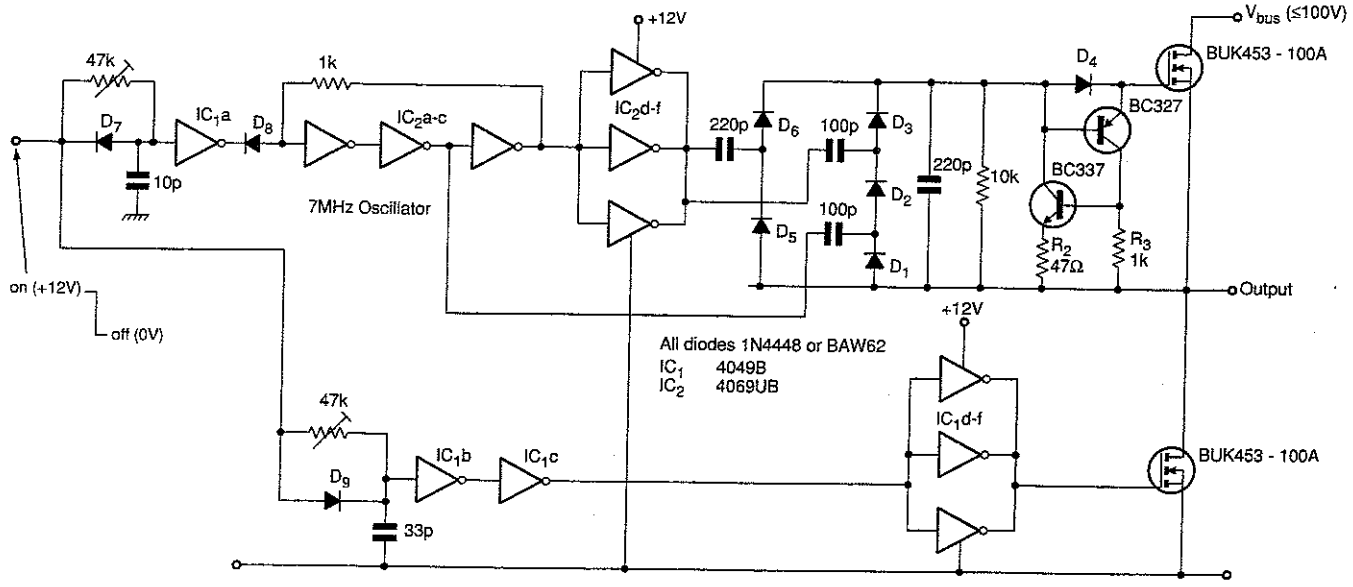


Fig. 6. This half bridge uses two low cost c-mos drivers, can operate up to 100kHz and the dead time can be varied.