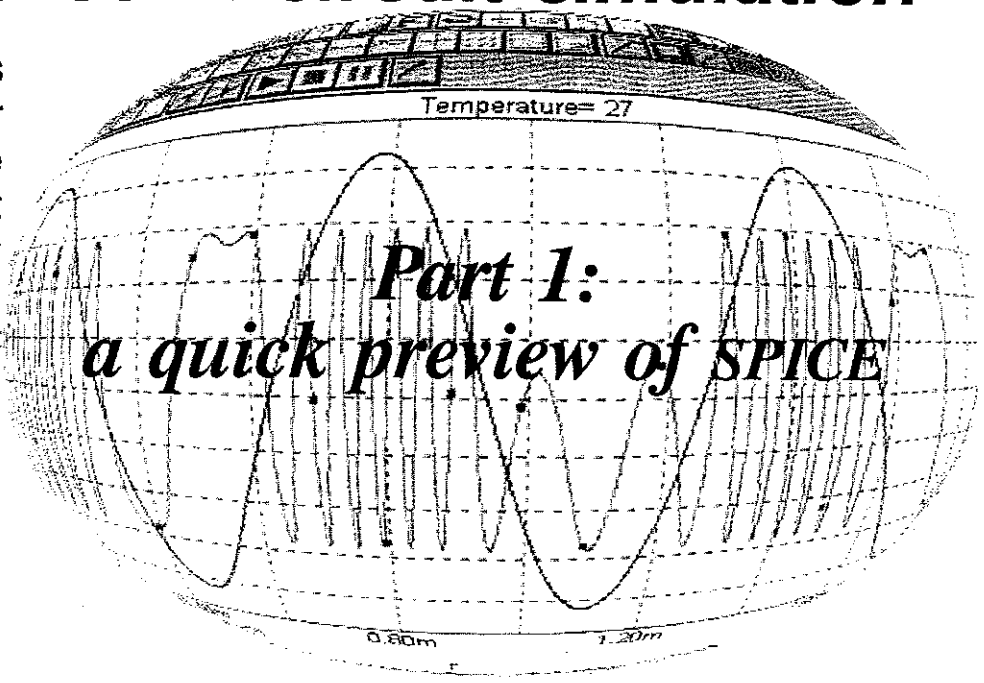
Circuit Simulation Course

ELEKTOR Electronics

HANDS-ON ELECTRONICS

a short course in circuit simulation



Part 1: a quick preview of SPICE

Following last month's focus on 'Software for circuit simulation', we now start a short (5-part) course in circuit simulation for beginners to this fascinating subject. The course is based almost entirely on SPICE, here contained in MicroCap V, a software package from Spectrum. A demo version of the program is available free of charge to anyone who asks for it either from Spectrum direct or from one of their distributors. A student version is also available (not free of charge). The demo version may also be downloaded from www page http://www.spectrumsoft.com. Spectrum's e-mail address is 103114.61@compuserve.com What's more, a version of the demo program is available from us at a small charge. See the Readers' Services page.

By Owen Bishop

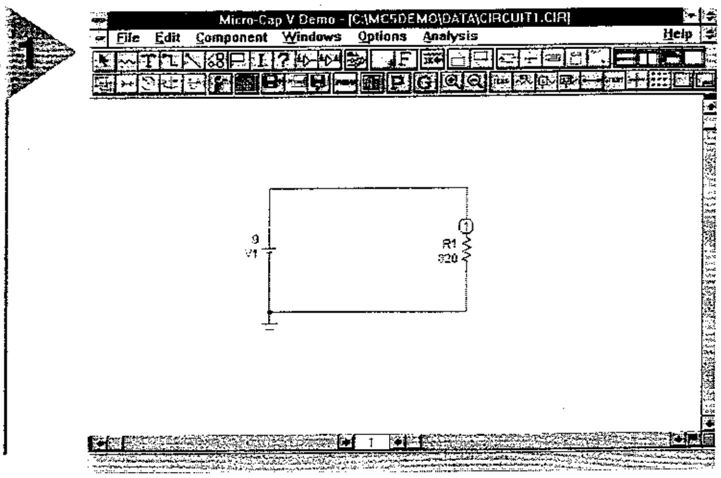
SPICE was developed as a designer's tool but, now that it has become so widely available, it can also be used in training and education. Instead of getting hands-on experience of electronic circuits on the workbench, the student, the engineer or the hobbyist can get an equal or even wider experience by putting hands on the keyboard. Compared with assembling and testing a circuit on the workbench or breadboard, computer simulation offers the advantages of:

- speed in 'assembly', circuit modifications and testing
- a virtual stock of an enormous range of components in all possible values
- no chance of burning out or damaging the components
- the equivalent of an unlimited range of test instruments, signal generators, oscilloscopes
- precision timing of events
- slowing down the circuit action makes it easier for the user to watch and record what is happening
- the subsequent opportunity to 'browse' through the test results

There are, of course, some pitfalls to be avoided when using a simulator and we shall look at some of these as we proceed.

The various commercial simulation packages nearly all have the same SPICE basis but differ in the details of circuit entry, analysis and display. The simulator used to illustrate this series is *Micro-Cap*. Formerly available as a PC-DOS program as far as version IV, it is now further improved as a Windows™ version, *Micro-Cap* V. The analyses in these articles can be run also on *Micro-Cap IV* or on most of the simulators published by other companies, though the operating routines and the presentation of results will differ. To make the explanations easier, the circuits are uncomplicated and can be run on 'Student' or 'Entry level' versions, and often on 'Demo' versions (such as the Demo version of *Micro-Cap V*), which permit the user to enter and analyse circuits of limited size.

This month, we begin with some elementary circuits to illustrate the major concepts of SPICE-based analysis. In the condensed instructions, actions that follow one after another are linked by an arrow →. This applies particularly to selecting from a series of menus and sub-menus. For example 'Component menu → Analog Primitives → Passive Components → Waveform Sources → Battery' represents a sequence of clickings on the items listed, as they appear.



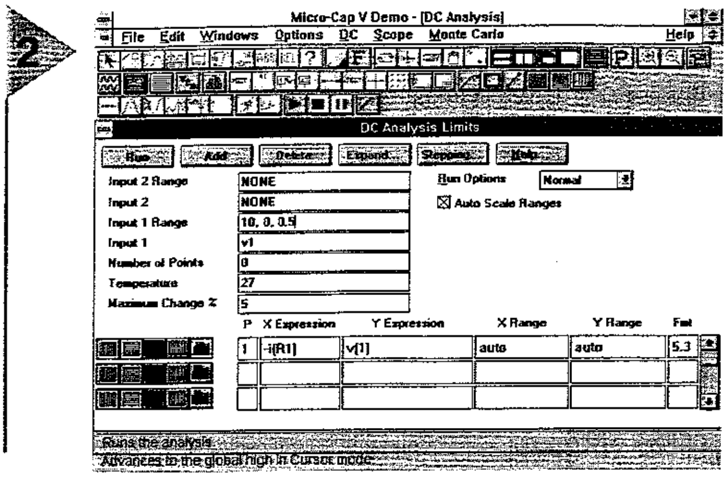


Figure 1. How to wire up the simple diagram of the first run of MC5.

SCHEMATIC EDITOR

When using SPICE itself, circuits are entered by typing in a *netlist*, which is a list of all the components, their values and the circuits nodes to which they are connected. The netlist includes instructions to the computer detailing the tests to be performed. Like other commercial simulators, *Micro-Cap V* (from now on referred to as MC5) provides for circuits to be entered as a schematic diagram, after which MC5 automatically converts this to its own form of netlist.

When MC5 is first run, the Schematic Editor window appears, blank at this stage except for two rows of control buttons at the top. The component cursor (pointer with zigzag symbol attached) is already enabled to draw resistors. Move it with the mouse, then click on a position to the right of the screen centre. The Component window appears, with the part name, R1, already allocated. You can change this by clicking on the box and typing in a new name. Be aware that names such as 'RC' and 'RE' may cause confusion later, as these may be taken to be parameters for models of semiconductor devices. Select VALUE and enter the resistor value, in ohms; in this example, '820'. Leave the MODELline unaltered, check the Display box to the right of VALUE (so that it shows a cross) to display the value on the schematic, and click on OK. The Component window disappears and a resistor symbol appears, with R1 and 820 beside it. These are green at the moment and at this stage can be deleted (by pressing the Delete key) if you have typed the wrong value. You can confirm this component by clicking somewhere on the screen, and it becomes blue with red name and value. But this also puts a second resistor on the screen. Only one resistor is needed here so, instead of clicking on the schematic area, click on the Component menu → Analog Primitives → Waveform Sources → Battery → back to the screen to place the battery left of centre. Press the left mouse key to obtain the symbol but, before releasing the key it, check that the symbol is the right way up - positive terminal on top. If not, rotate it by holding down the left mouse key and clicking the right mouse key repeatedly, until it is correctly orientated. Then release both keys. The Component window reappears with the component name, V1. Enter VALUE = 9. Check the Display box again.

Figure 2. The DC Analysis Limits window.

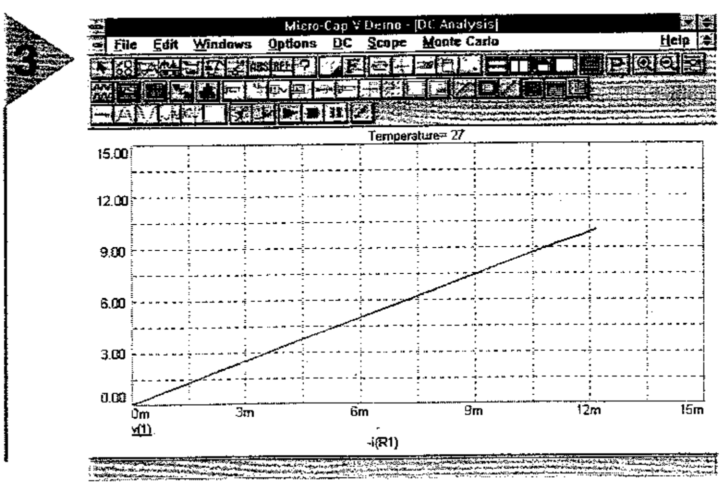
To wire up the circuit, click on the 4th button in the top row for Orthogonal Wire mode. Draw the two wires shown in **Figure 1**. All SPICE networks need to have the Ground node specified. Click on Component → Analog Primitives → Connectors → Ground → place the ground symbol on the 0 V line, as in the figure. This completes the schematic but, to add node numbers to the diagram, click the 8th button from the right on the 2nd row. The ground line is Node 0; the other node in this circuit is Node 1. Now to find out if MC5 knows about Ohm's law!

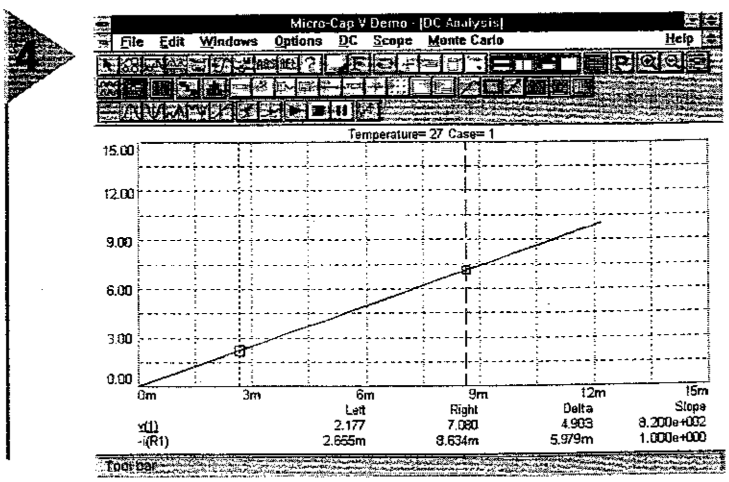
DC ANALYSIS

SPICE has three modes of analysis, and the first we try is DC Analysis. In this mode, all capacitors are open-circuited, all inductors are short-circuited, and all waveform sources are set to their initial values. Then one or two of the d.c. voltage (or current) sources are swept over specified voltage (or current) ranges and the node voltages and branch currents

Figure 3. The voltage vs. current characteristic is a straight line.

Figure 4. The voltage vs. current characteristic may be investigated more extensively in the [illegible]





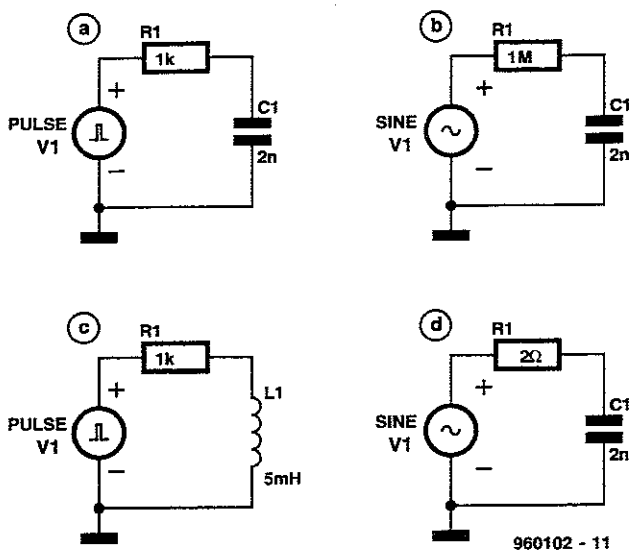


Figure 5. A number of circuits for analysis in the present series of articles.

calculated at each stage of the sweep. To see the effect of this, select the Analysis menu → DC Analysis. The DC Analysis Limits window (**Figure 2**) lets you set the conditions for the analysis, but first run the cursor around the various boxes and buttons on the screen, to observe their functions, which are displayed in turn at the bottom of the screen.

There is only one source in this circuit, so type its name 'V1' as Input 1 (replacing the word 'NONE'). A suitable Input 1 Range is 10, 0, 0.5. These numbers specify the final value, the initial value and the step value of the source, in volts. Note the reversed order of final and initial values. Note also that the value 9V specified for V1 on the schematic is not acted on in d.c. analysis. The maximum change of 5% automatically limits the amount of change at each step, should you have specified a step size larger than this.

Thinking ahead to the graph we wish to plot, resistance is volts/amps so, if the slope of the curve is to represent ohms, we need current on the *x*-axis and voltage on the *y*-axis. The X Expression is -i(R1), which means the negative of the current through R1. We use the negative to plot the graph with conventional polarity, since SPICE takes the direction of current flow to be from positive to negative *within the source*. This means that the current is not conventional current, but flows in the same direction as the electrons. Check the Auto Scale Ranges box so that an appropriate range for the axes is calculated by the software. Click on Run.

The plot of voltage against current is a straight line, showing the voltage is proportional to current (**Figure 3**). The slope of the curve is the resistance, which we can find by reading a pair of values on the graph. But we can investigate the curve more extensively by clicking on the 4th button in the top row to enable Cursor mode (**Figure 4**). There are two cursors, represented by vertical dashed lines, which can be moved sideways by clicking the left or right mouse buttons before moving the mouse. The point at which each cursor crosses the plotted line is picked out with a square, and its coordinates are tabled below the graph. The Delta column shows the difference between coordinates, and under Slope, the value of Delta in each row is divided by the Delta for the *x*-coordinates. This means that the Slope value in the upper row is volts/amps, the resistance value, which is shown as 8.200e+002, which equals 820Ω. This is as expected from the value we gave to R1 originally. These values are for a circuit at 27 °C, the standard temperature for SPICE analyses. This can be altered to any other value or swept over a specified range. Return to the schematic by clicking DC → Exit Analysis.

EXPLORING MC5

(1) Repeat the analysis. With the graph displayed, select Cursor mode as above and use top-row buttons 5 and 6 to measure *x* and *y* distances on the graph.

(2) Use bottom-row buttons 1 to 8 to move the cursors automatically to different locations on the curve; not many of these apply to the present curve but this is good practice for later.

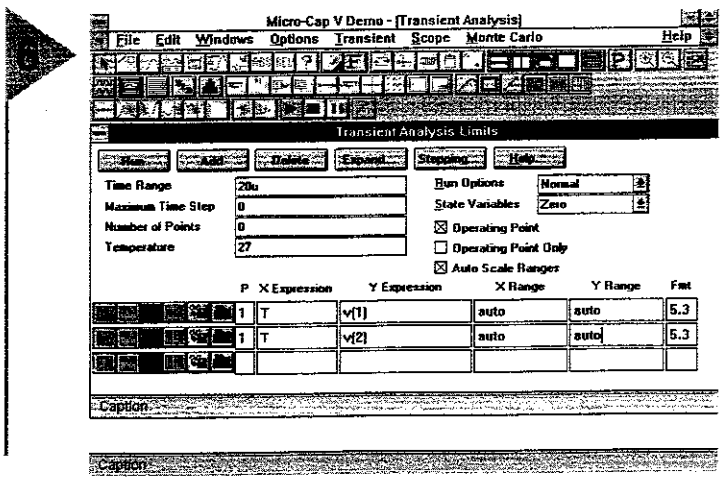
(3) Set up new d.c. analyses by altering the parameters in the DC Analysis Limits window. Alter the range of Source 1. Enter new X and Y Expressions, for example, try v(1) as the X Expression and -v(1)*i(R1) as the Y Expression to plot the power (in watts) dissipated in the resistor.

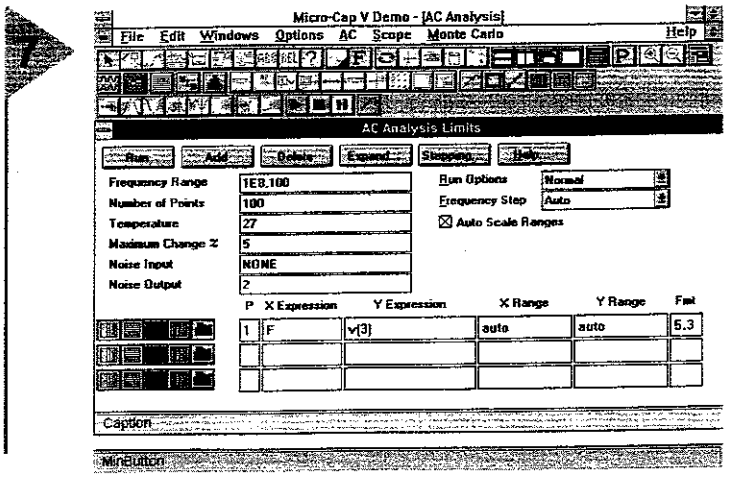
(4) Edit the schematic by changing the value of R1; click on top row button 8 (I), then on R1 → Component window → edit the resistor value (in SPICE, M is for milli- and MEG is for mega) → click OK →rerun the DC analysis.

(5) Redraw the

Figure 6. Parameters in the Transient Analysis Limits window.

Figure 7. Parameters in the AC Analysis Limits window.





schematic to put two resistors in series. Then plot the voltages for nodes 1 and 2. Voltages are relative to ground. To plot the voltage on a node relative to a second node, use the format v(*a*,*b*), the voltage at *a* minus the voltage at *b*.

To sum up, the cycle for such explorations, starting from the schematic, is: Analysis menu → DC Analysis → alter the parameters in the DC Analysis Limits window → Run → view graph → use cursors and measure distances → DC menu → Exit analysis → back to schematic → possibly edit it → repeat.

PROBE MODE

From the Analysis menu → DC Probe Analysis. This tiles the schematic with a small graph area. Clicking on one node or a succession of nodes causes the graph to display the voltage there as V1 is swept.

INVESTIGATIONS

Figure 5 shows some more circuits for analysis (answers next month):

(a) Here we use a second SPICE analysis mode, Transient Analysis. This calculates the way in which voltages and currents vary in time. The circuit must contain at least one time-varying source of voltage or current. Here we investigate what happens when the source delivers a single pulse. MC5 has its own pulse source but, to make these instructions applicable to other simulators, use the original SPICE independent voltage source and program it to produce the required pulse. On a new schematic editing screen (File → New → Schematic → OK), click on Component menu → Analog Primitives → Waveform Sources → V. After placing the symbol, its description in the Component window is PART = V1. Key in its VALUE = PULSE (0 1 1e-6 0). These figures define a pulse with low level 0 V, rising to high level 1 V after 1 μs (1e-6) delay, with 0 s rise time. Complete the circuit, then select Analysis → Transient Analysis. In the Transient Analysis Limits window set parameters as in **Figure 6**. Run. The graph displays the pulse and the p.d. across the capacitor. Note the exponential rise. Because we have not specified its length, the pulse lasts until the end of the plot. Transient menu → Exit Analysis → back to schematic. As in Exploration 4 above, edit the V1 pulse parameters to (0 1 1e-6 0 0 14e-6) which produce a pulse starting as before, but ending with a fall time of 0 s after 14 μs. Click OK. To see the effect of this, extend the time range to 30μs in the Transient Analysis Limits then Run. What happens?

(b) Repeat (a) but with a sine source. We use the same SPICE voltage source as above but replace the PULSE parameters with SIN (0 1 1k 0 0). These parameters specify, in order: offset (V), amplitude (V), frequency (Hz), delay (s), damping factor (s^{-1}). The damping factor THETA (Θ) produces an exponential change in amplitude, multiplying the amplitude at any instant by $e^{-\Theta(t-TD)}$, where t is the elapsed time and TD is the delay time. The parameter values quoted above produce a sine wave, with zero offset, amplitude 1 V, frequency 1 kHz, and no delay or damping. Change resistor value to 1MEG (1 MΩ). For a Time Range of 5 m (with T as the X Expression), plot the two node voltages, v(1) and v(2). Observe the amplitude and phase relationships between the waveform of the source and that across the capacitor. Try varying the frequency of V1, altering the Time Range to plot, say, 5 cycles. Explore the Cursor mode with these waveforms. By default, MC5 plots the graphs with 51 points. To increase the smoothness of the graphs, put Maximum Time Step = 10u (that is, 10 μs)

(c) Repeat (a) but with a 5 mH inductor in place of the capacitor. Explain the shape of the curve of the voltage across the inductor. Try other timings, or other values for resistor and inductor and observe their effects.

(d) The third SPICE analysis mode is AC Analysis. This calculates the fre-quency response of a circuit as the voltage source is swept over a prescribed range of frequencies. SPICE first finds the d.c. voltages and currents, then applies an a.c. signal, assuming that voltage or current variations are small and linear. Set up the *LCR* circuit. The frequency specified for the sine source is not important in the a.c. analysis, since it is swept automatically. You need to specify its amplitude and phase separately: extend the SIN statement of V1 to SIN (0 1 1k 0 0 AC 1 0). This specifies an a.c. signal of amplitude 1 V and zero phase delay. Click the Analysis menu → AC Analysis → AC Analysis Limits window (**Figure 7**). The Frequency Range is from 100 Hz to 100 MHz (1E8). Note the inverse order of specifying the range. Call for a plot of voltage across the inductor (v(3)) against frequency (F). Run. The graph shows a prominent peak at about 35 kHz, which is the resonant frequency of this circuit. Run the AC analysis with other values of L, C and R (better to change only one at a time, to observe the effects of change more clearly). Then run a Transient Analysis having set the frequency of V1 close to the resonant frequency. What do you notice about the amplitude of the voltage across the inductor?

[960102-I]

In passing ...

Armageddon?

Every sane citizen, whether acquainted with electronics or not, having witnessed the debacles that befell Philips and Sony in the 1980s in respect of their video recorder standards, will, no doubt, assume that we are no longer at risk from idiotic incompatible standards applying to consumer products.

For a while during the past month or so, it seemed, however, that there would be a hiccough in coming to a firm agreement on the digital versatile disc (DVD). It appeared that some of the original protagonists were dragging their feet regarding the paying of licensing fees to the (Japanese) patent holders. Particularly Philips and Sony felt that the development they had done on the new disc entitled them to a lower licence fee. This reluctance put in jeopardy the possibility of having DVD players on the market this coming Christmas.

Fortunately, common sense seems to have prevailed, because the latest news at the time of writing (September 1996) is that at least one company, Matshushita, will enter the Japanese market with two DVD players (Panasonic Type DVD-A100 and DVD-A300) this month. Similar products will become available in the USA towards the end of the year. Moreover, at the CeBIT show in Hanover in September, it was announced that Panasonic DVD players will enter the European market early next year. Price of the sets (in Japan) will be about £500 for the A-100 and just over £600 for the A-300.

According to statements at the CeBIT show, any fears that early customers may find themselves unable to record at a later stage are unfounded. It was admitted, however, that there are still problems with the development of the LSI chips for MPEG2 decoding, but that specifications that deal with backward compatibility are definite.

It was learned from other sources that the LSI chips may not become available until the end of 1998. Whether this is a political/commercial ruse only time will tell.

[960309]

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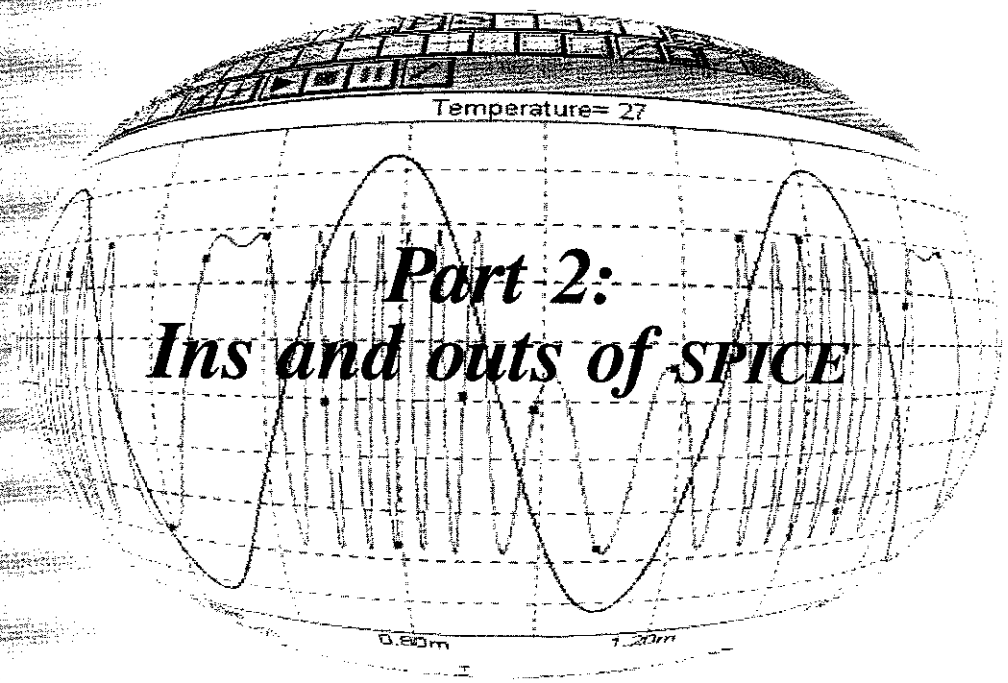

Part 2: Ins and outs of SPICE

Last month's article gave a quick preview of **SPICE**. This is followed this month's by a close look at a common-emitter amplifier and, based on this, an illustration of ways of putting data into a **SPICE** simulation and getting data from it.

By Owen Bishop

COMMON-EMITTER AMPLIFIER

The common-emitter amplifier in **Figure 8** was designed to operate on 9 V with a quiescent output voltage of about 4.5 V and to pass signals in the audio range (30 Hz -20 kHz). Select the BJT transistor first, clicking on Component → Analog Primitives → Active Devices → NPN. Before placing the transistor in the centre of the screen, use the right mouse button to turn it the right way up. When it is placed, the Component window asks for its MODEL. Select 2N2222A from the panel on the right. Check the Display Box. The remainder of the circuit is assembled as described last month; for V1, VALUE = 9; for V2, VALUE = SIN (0 0.02 500 0 0). This is a 500 Hz sine wave, amplitude 0.02 V, offset 0 V, zero decay, zero phase delay. To see the specification of the transistor, click on the small button at the bottom right of the screen. This displays the Text Screen on which is the .MODEL definition for the transistor:

.MODEL 2N2222A NPN (IS=8.57646P BF=168.002 ...)

2N2222A is the model name, NPN is its type, and the brackets contain a list of its parameters. The first two indicate that the saturation current I_S is 8.57646 pA, and the forward gain β_F is 168.002. There are 21 other parameters, all of which are used, along with state variables (relevant network voltages and currents), in a set of equations by

```
                DC Operating Point Values
                DC Operating Point Voltages
Node  Voltage  Node  Voltage  Node  Voltage  Node  Voltage
   1      9      2      4.3    3      1.06    4      1.66
   5      0      6      0
                Bipolar Junction Transistors
                Q1

IB          1.283-005
IC          1.04e-003
VBE         6.07e-001
VBC         -2.64e+000
VCE         3.25e+000
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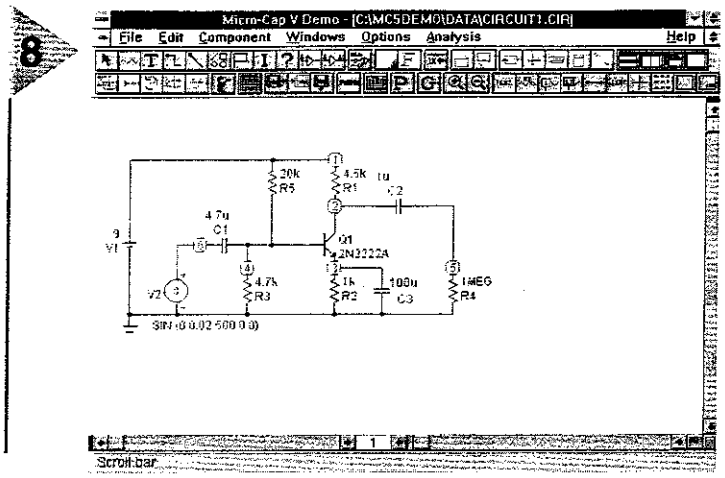


Figure 8. Common-emitter amplifier operating from a 9 V line. Its output is 4.5 V.

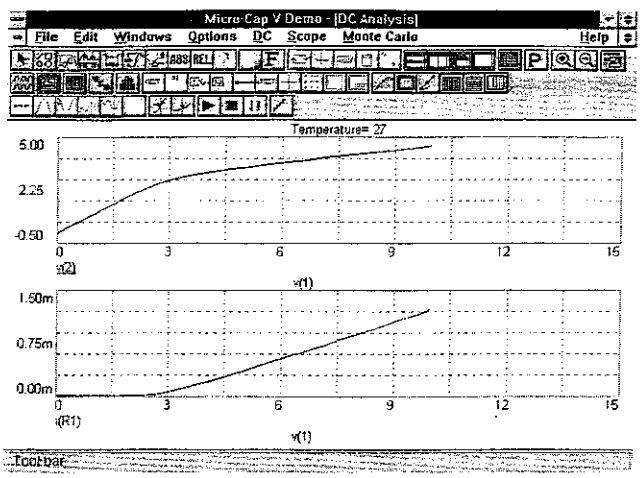


Figure 9. Current plots on different scales.

which the BJT is modelled and its behaviour predicted. Now we look at some the output data that can be obtained from this amplifier.

DC ANALYSIS

Click on Analysis → DC Analysis to obtain the DC Analysis Limits window. Input 1 Range of 10, 0, 0.5 is already displayed and is satisfactory. For Input 1, enter V1, the d.c. source. Check the Auto Scale Ranges box. As the d.c. source is swept from 0 V to 10 V, we will plot two variables, the emitter voltage at Node 3 and the collector current. Accordingly, the first plot has X Expression v(1), and Y Expression v(2), while the second plot has X Expression v(1) and Y Expression i(R1). A '1' in each of the P boxes causes both plots to be made on the same grid. In the resulting plot, it is seen that v(3) rises with increasing v(1) but the current appears to be zero. This is because the current is being plotted on the same scale as v(3) but, as it is only a few milliamps, there is no discernible change. One way to display the current effectively is to change its Y expression to i(R1)*1000. This multiplies it by 1000 before plotting. The result of this is a pair of curves that are almost coincident, since $v(3) = i(R2) \times R2 = i(R2) \times 1000 \approx i(R1) \times 1000$. Another way of displaying the current is to plot it on a separate grid. Leave the '1' in the P box in the first line, but enter a '2' in the P box of the second line. Now we obtain separate plots on appropriate scales (**Figure 9**). The graphs show that when the supply voltage is 9 V, the collector voltage is close to 4.5 V and the emitter current is 1 mA, as specified in the original design.

TRANSIENT ANALYSIS

In the Transient Analysis Limits window, key in 10 m as the Time Range, 10 u as the Maximum Time Step, and check the Operating Point Only box. SPICE always determines the d.c. operating point as the first step in an analysis. It sets the initial values on which a Transient Analysis is based. Here we have asked it to determine the operating point and then stop. No graph appears when we Run the analysis. The results we have asked for are displayed in the Numeric Output window. Display this by clicking on the 3rd button in the middle row. A table of results is displayed as shown at the bottom of the previous page.

These are the quiescent values to which the node voltages will settle in the absence of an input signal. In particular, the emitter voltage is 1.06 V, in agreement with a 1 mA emitter current, and the base voltage is 1.66 V, giving a 0.6 V base-emitter drop. Having been satisfied that the circuit has a correct quiescent state, click on Transient → Limits, then deselect Operating Point Only, and select Operating Point and also Auto Scale Ranges. In this transient analysis, we look at input and output voltages, by plotting two graphs on one grid. Both P boxes contain '1'. The X Expressions are both 'T' (for 'time') and the Y Expressions are v(6) and v(5) respectively. The plot shows v(5) as a sine wave, amplitude 2.55 V (use the Vertical Measure mode, top row, button 6), 180° out of phase with v(6). We have specified the amplitude of v(6) to be 0.02 V, so the amplifier gain is 2.55/0.02 = 12.6. Again, v(6) is too small to show clearly on the same scale as v(5). Either multiply v(6) by a factor such as 10, or plot them on two grids.

Graphs give a useful overall view of the waveforms but sometimes we might wish to know the voltage at a given moment with a degree of precision. The Vertical and Horizontal Measure modes are very helpful but, for the most accurate results, we use a table of the actual values from which the graphs are plotted. To obtain this, enable the Numeric Output mode by clicking on the 4th button in the row to the left of the P box. Decide on how many points are required (say 200) and enter this in Number of Points. Run. After the graph is plotted, click on the Numeric Output button (3rd button, middle row). The DC Operating Point data is displayed as before, followed by transistor voltages and some of its parameters. Then comes a table of voltages against time for all 200 points in the Time Range. This data can be printed out or saved to a file, or you can copy it out by hand if you need just one or two points.

AC ANALYSIS

Use this to find the response of the amplifier at different frequencies. The first thing is to edit V2 to include its a.c. parameters, v value = AC 0.02 0. We have given the swept signal

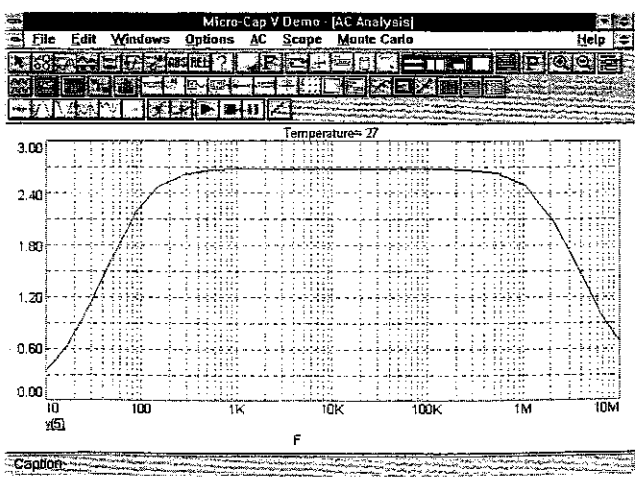


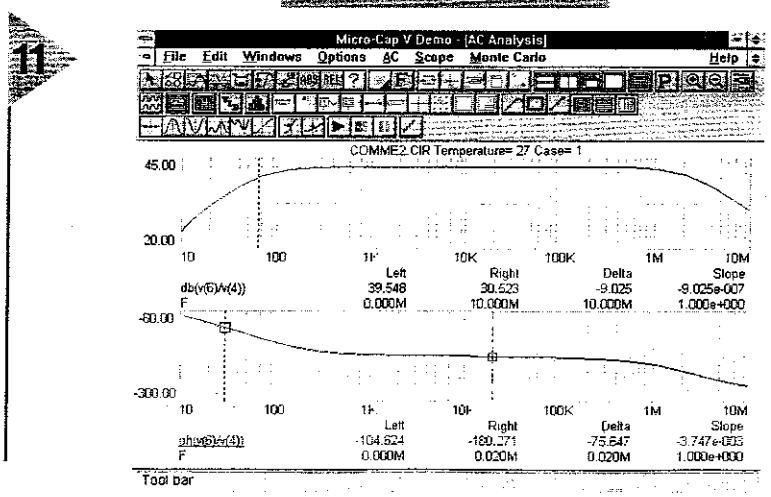
Figure 10. Amplifier response (voltage vs. frequency) at different frequencies.

the same amplitude as in the previous tests. In the AC Analysis Limits window set the Frequency Range to 1E7, 10, which means from 10 Hz to 10 MHz. Only a single graph is required so, if the P box of the second row contains a '1', replace it with a blank. For the graph plot output voltage, v(5), for the Y Expression against frequency (F for the X Expression). The result is **Figure 10** which shows maximum output between 800 Hz and 200 kHz, rolling off at frequencies below and above this range. Alternatively, you could plot gain v(5)/v(6) against frequency and obtain a graph

```
* COMMON-EMITTER AMPLIFIER
V1    1    0    9
V2    6    0    SIN (0 0.02 1K 0 0)
Q1    2    4    3    QONE
R1    1    2    4.5K
R2    3    0    1K
R3    4    0    4.7K
R4    5    0    1MEG
R5    1    4    20K
C1    6    4    4.7U
C2    2    5    1U
C3    3    0    100U
.MODEL   QONE   NPN   BF=150   RB=120
VAF=105 CJC=5P
.TEMP 20
.OP
.TRAN 10E-6 0.005
.PLOT TRAN V(5)
.END
```

of the same shape. It is more usual to plot gain on a decibel scale, for which the Y Expression is db(v(5)/v(6)). At the same time, as a second graph (a '2' in the P box), we plot the phase of the output signal relative to the input signal entering the Y Expression as ph(v(5)/v(6)). The result is **Figure 11**, which is displayed in Cursor mode. The signal level is 42.5 dB for most of the frequency range, falling to 3 dB less than this at 65 Hz. It is necessary to alter C_1 to make the –3 dB point at 30 Hz. Phase is –180° over a large part of the audio range (1 kHz to 20 kHz), decreasing to –105° at 30 Hz. This is a reasonably even phase response.

Figure 11. Amplifier response on a decibel scale. The lower graph shows the phase of the output signal relative to that of the input signal.



SPICE NETLIST

An alternative way of entering a circuit is to type in a SPICE netlist. Some users may find it easier to do this than to manipulate the symbols, names and values of the Schematic. The netlist does not present such a clear picture of the connections between components but I, for one, find a netlist much easier to edit than a schematic. In the first column, for example, is the netlist of this month's circuit:

The title line begins with an asterisk so that it is ignored by SPICE. Next come the Element Statements which is a list of components, the nodes to which they are connected, and their values. From this we see, for example, that d.c. source V1 is connected to nodes 1 (positive first) and 0 and its value is 9 V. V2 is connected to nodes 6 and 0, and its operation is defined as we have previously noted. A BJT transistor is coded as Q in SPICE, then follow the nodes to which its collector, base and emitter are respectively connected. The model name QONE is an arbitrary name referring to the model statement later in the list. The model statement begins with .MODEL, followed by model name (QONE), NPN to indicate its type, and then a list of parameters. It is not necessary to assign values to all 40 parameters because default values are used for those left undefined. Here we make the forward gain 150, base resistance 120 Ω, forward Early voltage 105 V and the capacitance of the base-collector junction 5 pF. The .TEMP Control statement sets the running temperature to any chosen value, 20 °C in this example instead of the SPICE standard temperature of 27 °C. The statement .OP directs SPICE to perform a d.c. operating point analysis. This is virtually an essential preliminary to a Transient Analysis, as explained above. The statement .TRAN 10E-6 0.005, asks for a Transient Analysis, sampled at 1 μs intervals for 0.005 s (5 ms). The .PLOT statement asks for the values of v(5) to be plotted. Finally, the .END statement is a mandatory part of any SPICE netlist.

This netlist can be typed directly into MC5. Run MC5 and, when the opening window appears, click on File →New → Spice/Text → OK → type in netlist. Or type the netlist in with a word-processor such as MS Works, then copy it to the Clipboard. Run MC5 as above and, after OK, click on Edit → Paste. Click on Analysis → Transient Analysis. The Transient Analysis Limits window appears with the Time Range already set to 0.005 and the number of points set to 501 (equivalent to 1 μs intervals). The temperature is already set to 20 °C and the Operating Point box already checked. Run the analysis to obtain the plot. If you click on the Numeric Output button, you see the d.c. analysis similar to that described earlier. Click on Transient → Exit Analysis to return to the netlist display, which you can then edit or extend. There is no space here to go further into the details of SPICE netlist syntax, but enough has been shown to demonstrate this alternative way of making input to MC5.

INVESTIGATION 2

The amplifier was intended to pass audio frequencies above 30 Hz, by which we mean that the output amplitude at 30 Hz should be no more than 3 dB below its maximum at higher frequencies. Instead, it is about 7.5 dB down, giving a loss of bass tones. Find out what change must be made to the capacitance of one of the capacitors to give a roll-off of –3 dB at 30 Hz.

INVESTIGATION 1 (ANSWERS)

Last month's circuits are repeated in **Figure 12.** Circuit (a) demonstrates the charging and discharging of a capacitor by a constant voltage source. It is tested with a 1 V pulse starting at t = 1 μs and ending at t = 14 μs. As soon as the pulse begins, the p.d. across the capacitor, v(2), rises exponentially to 1 V, according to the equation $v_c = v(1-e^{-t/RC})$, where v is the pulse height = 1 V. When the pulse ends, v(2) falls exponentially from 1 V to 0 V according to the equation $v_c = v(1 + e^{-t/RC})$.

In circuit (b), when the source is a 1 kHz sine wave, amplitude 1 V, the signal across the capacitor is a 1 kHz sine wave, amplitude 0.074 V, lagging 90° behind the source. At 1 kHz, the impedance of C_1 is $1/2\pi fC$ = 79.6 kΩ. In series with R_1 this forms a potential divider, total resistance 1079.6 kΩ. The

proportion of the source voltage (1 V) developed across C_1 is 1×79.6/1079.6 = 0. 074 V, as found in the analysis. Note how the average value of the waveform across the capacitor gradually drops; on the first upward swing of V1 the p.d. across the capacitor swings up to 0.74 V, giving an offset of 0.37 V. But gradually this charge leaks away, the average value (or offset) becoming 0 V.

At the beginning of the pulse in circuit (c) the sudden rise in p.d. across the inductor induces an equal and opposite e.m.f. **Figure 13**), but when there is no further change in p.d. from the source, there is no induced e.m.f. and the p.d. across the inductor falls. Conversely, a sudden fall of p.d. at the end of the pulse induces a negative spike, and again the p.d. gradually falls to zero. With larger inductors there is a slower return to zero so that, for 200 mH or more, the p.d. across the inductor almost follows the pulse. With smaller inductors there are smaller, short-lived spikes.

Circuit (d) illustrates several features of a resonant circuit. With component values as specified, the resonant frequency is $1/\{2\pi\sqrt{(LC)}\}$ = 35.6 kHz. On the a.c. analysis plot of the inductor p.d.,v(3), against frequency, there is a sharp peak at this frequency. The peak reaches 18.2 V. The voltage falls to zero at lower frequencies and to 1 V at higher frequencies. Increasing R_1 reduces the height of the peak (dampens the response); if R is 5 kΩ or more the peak disappears and then the plot takes the form of the output of a high-pass filter. As expected from the equation, increasing C_1 or increasing L_1 both reduce the resonant frequency.

Figure 14 explains how it is possible for the p.d. across the inductor to rise to 18.2 V or even higher (it rises to 60 V when the inductance is 1 H) although the source amplitude is only 1 V. The waveform across the capacitor lags 90° behind the source but the waveform across the inductor leads the source by 90°. Consequently, the capacitor and inductor waveforms are 180° out of phase and largely cancel each other out, instant by instant.

Figure 14 also shows the amplitude of both waveforms is gradually increasing. This is because, at each cycle of the source, a little energy is fed into the circuit. Since the swings in p.d. across the capacitor and inductor are of the same frequency as the source, the energy in the circuit (in the form of electric charge on the capacitor, or magnetic field in the inductor) increases. A real circuit would reach an equilibrium in which the energy added each cycle would be equalled by energy escaping from the capacitor, inductor and resistor in the form of heat. This feature is not modelled in the SPICE circuit and so the voltage swings quickly reach amplitudes which would destroy real components. It is possible to model such happenings but this has not been done in these analyses. This is a reminder that a simulation models only those aspects of reality that are written into it. If it is not programmed intelligently, it may sometimes give false results.

Incidentally, the two curves in Figure 14 are distinguished by marking one of them with tokens. This is done automatically by clicking on the 4th button from the right in the bottom row. This feature is useful if graphs are to be reproduced in black-and-white, as in a book or magazine.

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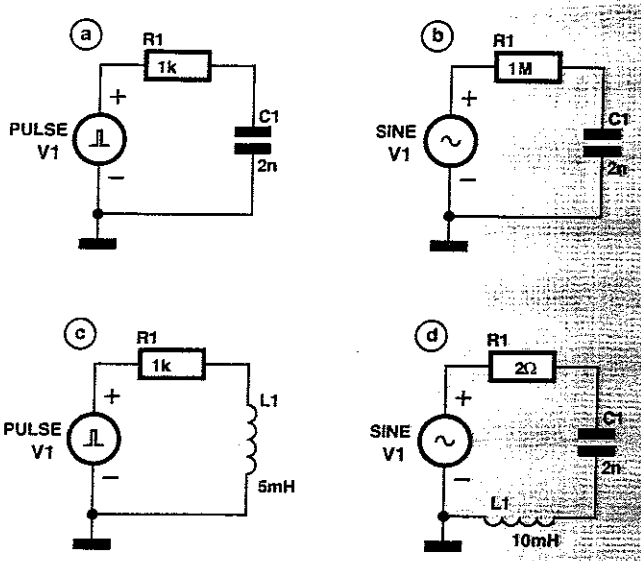
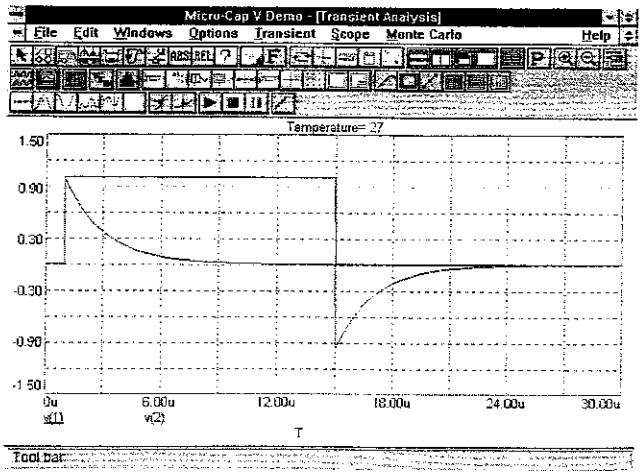


Figure 12. Repeat of Figure 5 in Part 1: A number of circuits for analysis by the reader.

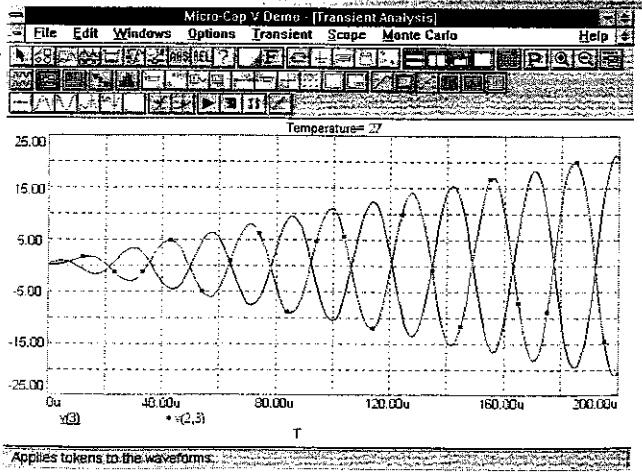
Figure 13. A sudden rise in p.d. across an inductor produces an equal but opposite e.m.f.

Figure 14. Illustration of how a p.d. across an inductor can rise to many times the level of the source voltage.

13

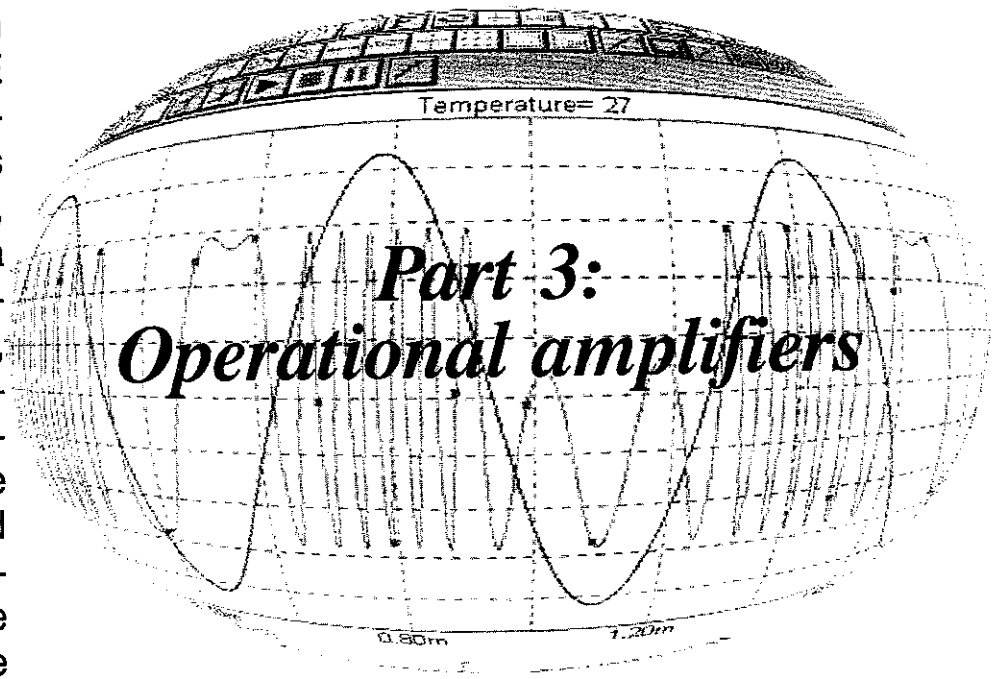


14



HANDS-ON ELECTRONICS

a short course in circuit simulation



Part 3: Operational amplifiers

As we have seen in Part 2, the SPICE primitives, such as resistors, capacitors and voltage sources, are defined in a netlist by an appropriate code letter (R, C, V) followed by identifying numbers or letters, then by node connections and value. The exact syntax depends on the element and is more complicated for voltage sources and similar elements.

MODELLING

A number of elements take MODEL names. In SPICE2, these are the elements with the code letters, D, NPN, PNP, NJF, PJF, NMOS and PMOS, whose identity is obvious from their codes. SPICE3 has a few more such elements including voltage and current-controlled switches and MESFETs. All of these elements need to be given model names, such as QONE, or 2N2222A, such as we used in netlists quoted last month. These names are quite arbitrary, for the convenience of the user. If several transistors are given the same model name, a single .MODEL statement in the netlist suffices to define the behaviour of all these transistors. If there are two or three different transistor types in the netlist, they are given two or three different model names and we need a .MODEL statement for each model name. The models referred to in these statements direct the computer to follow built-in sets of equations or algorithms which model the behaviour of that type of element in accordance with various parameters specified in the statement.

Neither SPICE2 nor SPICE3 has an op amp primitive. If you are using SPICE, rather than one of its commercial enhancements, you model an op amp as a sub-circuit. The simplest of these is a voltage-controlled source (**Figure 15**) which can be considered as an ideal model (ideal in the sense of being theoretical, not in the sense of being the best practical op amp for the job) because it has infinite input impedance, zero output impedance, and has a very high open-loop gain. The subcircuit to define such an op amp model is:

```
.SUBCKT OPAMP 1 2 3
E1   3 0 1 2 1E6
.ENDS OPAMP
```

The .SUBCKT line specifies the subcircuit name and lists the node numbers of the input and output terminals, as included in hexagons in **Figure 16**. Next comes the subcircuit netlist which, in this case, comprises only one component. E is the code for a voltage-controlled voltage source. The E1 line lists the node connections of the voltage source in order n+, n-, nc+, nc-, and the gain parameter. The output at n+ equals the difference between the voltages of the nc+ and nc- (control) inputs multiplied by the gain parameter. In this example, it is 1×10^6, equivalent to the open loop gain of the op amp. This is one of the simplest possible subcircuits, consisting as it does of only one element. Subcircuits may have a virtually unlimited number of elements.

In the main netlist below, which is the netlist of an inverting amplifier based on the op amp subcircuit, the name of the op amp begins with X, the code used for a subcircuit, followed by numbers or letters to differentiate between op amps if there is more than one. The subcircuit is called by its subcircuit name:

```
*INVERTING AMPLIFIER
XOA  0 2 1  OPAMP
R1   1  2  100K
R2   2  3  10K
R3   1  0  10M
V1   3   0  SIN (0 1 1K 0 0)
.END
```

You could enter this into MC5 as a netlist or as a schematic (**Figure 16**). Obtain the source E1 by Components

By Owen Bishop

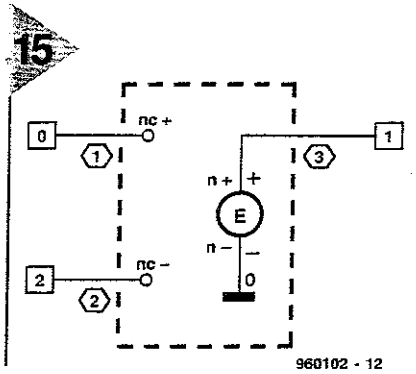


Figure 15. The numbers in the hexagons are listed in the SUBSKT line that specifies the subcircuit name.

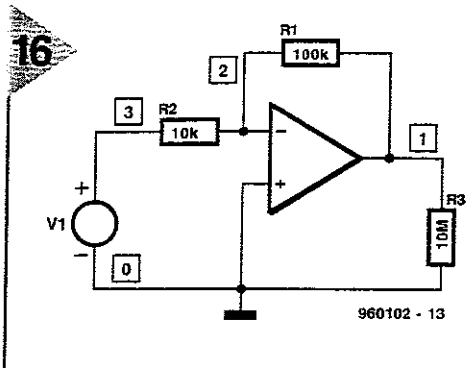


Figure 16. Circuit diagram of the inverting amplifier.

Analog Primitives Dependent Sources VofV. After placing it, enter VALUE = 1E6 in the Component window. R3 acts as a high-impedance load. When the circuit is complete, check its action by running a Transient Analysis for 5 ms and plotting both V(3) and V(1) against Time. Confirm that it acts as an inverting amplifier with closed-loop gain of 10, as illustrated in **Figure 17**. Observe the effects of varying R1 and R2, and the amplitude and frequency of V1.

Although this model behaves perfectly well with certain resistor values and input, it is not difficult to make it produce nonsensical results. Set R1 and R2 to give an open-loop gain of, say, ×100 and set the amplitude of V1 to 25 V. The output amplitude is 2500 V, which is obviously impossible. Change R3 to 2Ω and you can draw as much as 5A from its output at 10 V. At 1 MHz, the open loop gain is still ×106, whereas with a real op amp it would have dropped to around ×1 at that frequency. Some of these deficiencies can be eliminated by adding further components to the subcircuit. Add resistors to simulate input and output impedance, as well as input bias current. Add a capacitor to reduce the gain at high frequency. Add diodes to limit the output voltage swing to realistic values. The more additions, the more accurately it models a real op amp. On the other hand, the more additions, the longer the computer takes to calculate its behaviour in each cycle of the analysis.

At the other extreme, it is possible to model an op amp exactly with a netlist which includes all the components of an actual op amp circuit. It will have about 30 nodes and to include even one such detailed model in a netlist increases analysis time significantly. A compromise is reached by designing a netlist which does not follow the layout of the actual op amp circuit but, by including controlled voltage sources (not present in real op amps), behaves almost exactly like a real op amp, even though the number of elements and nodes in it are fewer than 20.

MC5 OP AMPS

MC5 and most of the other enhancements of SPICE have their own inbuilt op amp models. There is no need to invent netlists to simulate an op amp. An op amp is called up simply by using the op amp model and defining its parameters, just as you would call up a SPICE transistor model. Examples of these are provided in the MC5 file OPAMP1.CIR, which is loaded in a new schematic window by File Open opamp1.cir. This is a demonstration of 3 different op amp models, all fed with a single pulse from a generator. The op amps are connected as voltage followers, so their outputs should theoretically follow the input exactly. Run a Transient Analysis to see what happens (**Figure 18**). The square input pulse and the square pulse from the output of op amp 01 (the ideal model) are coincident. This might be thought to be just what is expected, but note that this is a pulse of very short duration and a real op amp could not follow such rapid voltage changes because of the limitations of slew rate. The two-pole model (02, hollow square tokens on the curve) has a more realistic response but fails to reach 10V before the pulse ends. The Boyle model (03, cross tokens) has a sharp initial upsurge as the pulse begins, allowing it to reach 10 V just before the pulse ends. Here we have three models with three degrees of resemblance to a real op amp.

Returning to the Schematic window, look at these models in more detail by reading their model statements on the text screen (click on the bottom right corner of the Schematic window). The models are named 01, 02 and 03 respectively and they all have the same model type, OPA (meaning operational amplifier). Their parameters begin with a statement of level: 1, 2 or 3. Model 01 is level 1 and has the fewest parameters; consequently, it is

Figure 17. Schematic of the diagram in Figure 16.

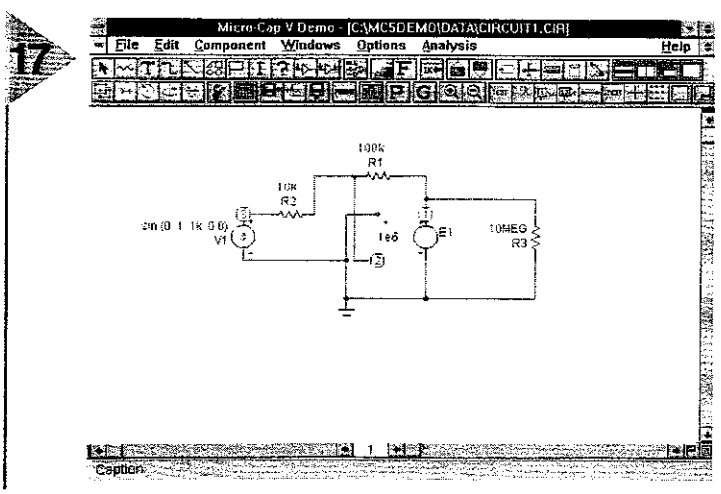
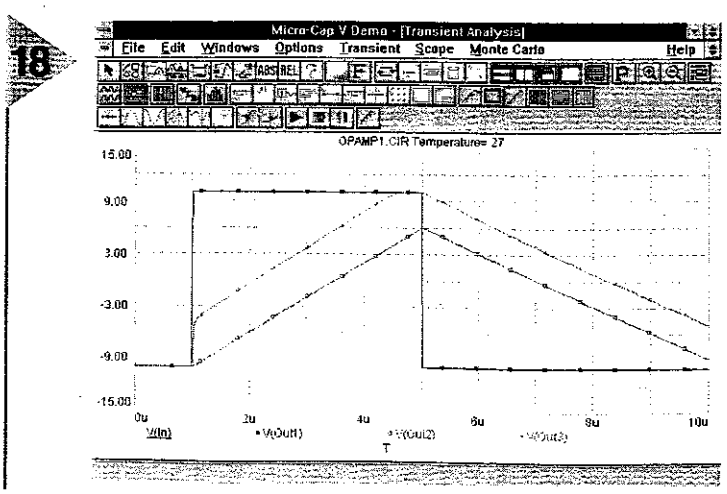
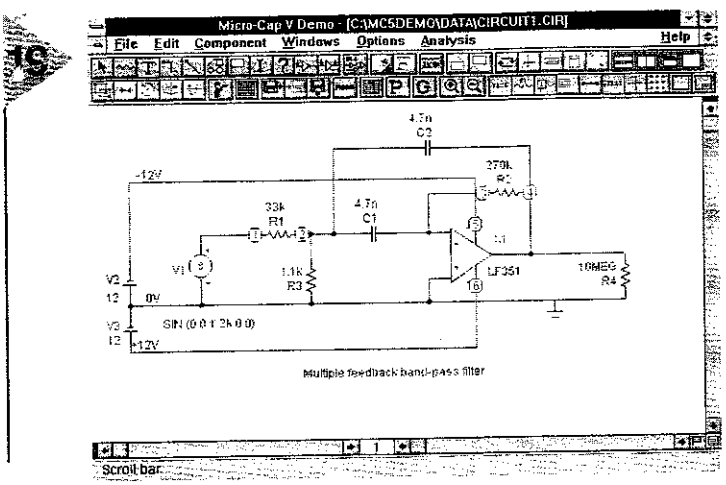


Figure 18. Transient analysis to follow the action of an op amp.





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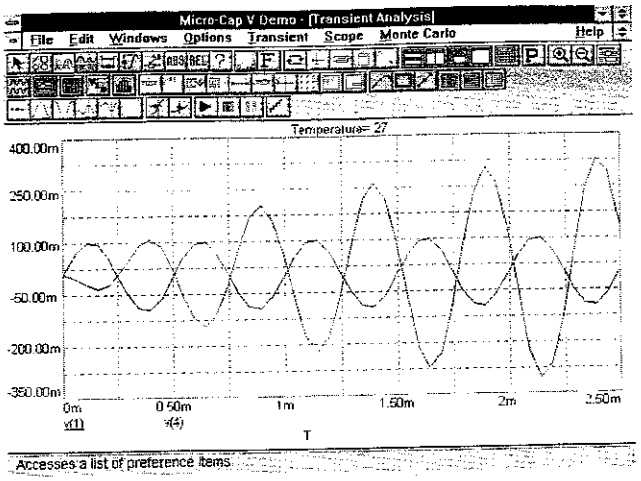


20

Figure 19. Active filter based on an operational amplifier.

Figure 20. Transient analysis to verify that the active filter is working correctly.

the least realistic but the fastest to run, so it is useful, but in a limited rage of situations. Its parameters specify only open loop gain, and output impedance under DC and AC conditions. Model 02 specifies the same parameters as 01 and, in addition, positive and negative slew rates, gain bandwidth and phase margin. The importance of modelling slew rate has already been noted in Fig. 18. Finally, model 03 has the same specification as the two previous models and also offset voltage, input bias current and common mode rejection ratio.

Try editing some of the parameters of these models and observe how their action is affected. Also edit the schematic to replace the pulse generator with a sine generator; vary its frequency. Finally, edit the circuit to obtain some of the standard op amp configurations, such as inverting amplifier, non-inverting amplifier, and integrator. Discover how well (or how badly) these circuits work.

Given a set of data sheets which specifies the parameters, it is possible to construct an op amp model that has the characteristics of any given manufacturer's type. MC5 has a library of models which may be used when high precision modelling is required. For example, click on Component → Analog Library → Op Amp → LF0000- → LF147- → LF347. An op amp symbol appears on the cursor which you can position as required. Click on the Select Arrow, then double click on the op amp symbol. In the Components window, check the Display box so the op amp type number is displayed on the schematic. You can optionally check the Display Pin Names box to have the names of all the op amps pins displayed on the schematic, but they often make it difficult to see the connections clearly. To examine the parameters of the .MODEL statement, click on Edit Add Model Statements bottom right of window Text Area with model statements displayed. Here we find, among other things, that the DC open loop gain of the LF347 model is ×105, its input bias current is 50 pA, and its input offset voltage is 5 mV.

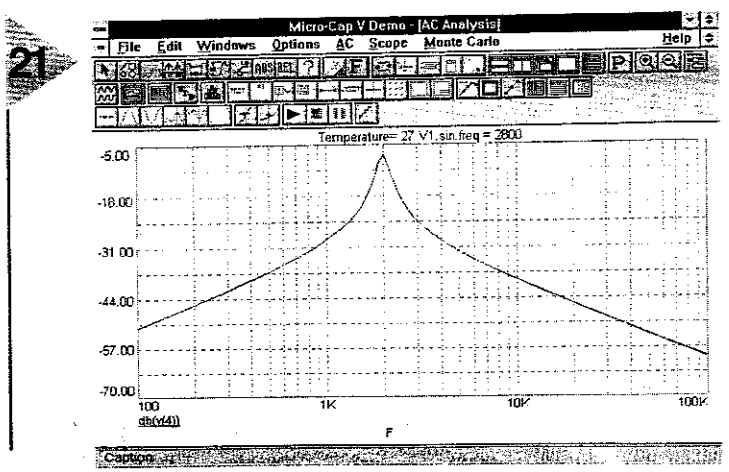
ACTIVE FILTER

Figure 19 is an active filter based on an op amp. With only one op amp in the circuit, there is no need to worry about how long the analysis will take. So we can use a level 3 model based on a particular type. We have chosen the LF351, an op amp with JFET inputs and a high slew rate (13 V/μs). The circuit operates by multiple feedback to produce a band-pass filter. The values in Fig 20 are calculated for a centre frequency f_c of 2 kHz, but using the nearest standard values instead of the exact calculated values. Using standard values for resistors and capacitors is convenient, but to what extent does this move the filter off the required f_c ? This filter can be tuned to a given fc by adjusting R3, so what value must R3 have to bring fc exactly to 2 kHz? The component values are calculated to give a filter with 250 Hz bandwidth and a gain of ×4, and we must confirm that it meets these specifications.

First set up the circuit; for the op amp, go to the Analog Library as described above. Note that the op amp symbol is drawn so that the (+) input is above the (-) input when the op amp 'points' toward the right. The circuit layout is clearer with the op amp turned the other way up (press the right mouse key a few times), but now

Figure 21. AC analysis of output amplitude variations with frequency.

Figure 22. Placing the cursors appropriately enables the two cut-off frequencies, and thus the bandwidth, to be read.



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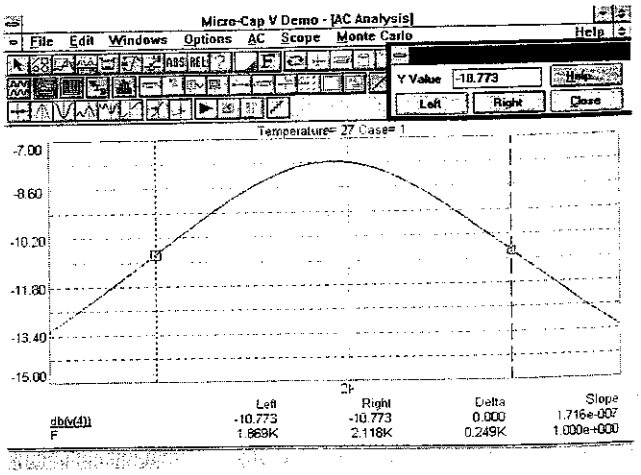
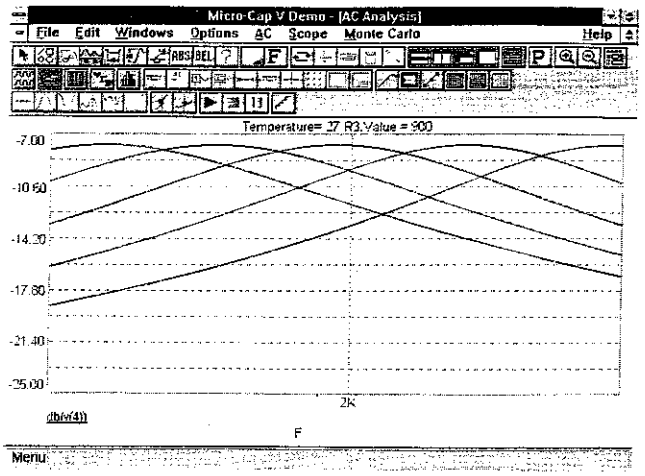


22



Figurer 23: Curves obtained by sweeping component values over a given range in steps of a given size.

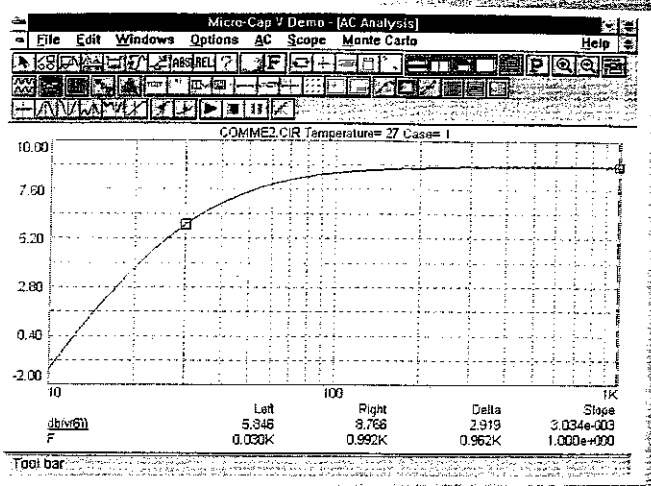


Figure 24: Low-frequency response of an amplifier, answer to the investigation in Part 2.

we have to invert the battery connections. To remind us of this, we have labelled the power leads. Click on the text 'T' key, then click on the point where the text is to be printed. An entry panel appears; type in the text, then OK.

Check that the circuit is working properly by running a Transient Analysis. A suitable time range is 2.5 ms. Plot V(1) and V(4) against time. The result is **Figure 20**; The amplitude of V(1) is constant, but that of V(4) increases steadily. Does this trend continue or is it simply due to the capacitors gaining charge during the first few cycles? Running the analysis for 20 ms shows that the amplitude of V(4) stabilises at 346 mV after about 4 ms, a gain of ×3.45, rather lower than the design specification.

To investigate how output amplitude varies with frequency, try an AC analysis. First add 'AC 0.01 0' to the parameters of V1. Set the Frequency Range to '100k,100', the number of points to 1001. To obtain a smooth curve, under Frequency Step, select Fixed Linear. This allows 1001 points to be plotted, instead of the number being limited by the 5% Maximum change. Check the Auto Scale Ranges box. Plotting db(V(4)) against F, gives **Figure 21**. This is shown here in Cursor mode and we have clicked the 'Advance to Global High' button, and clicked the left mouse key to bring the left cursor to the peak of the response curve. This is read as 1.990 K, which is close to the required value of 2 kHz. The magnitude is –7.773 dB. To find the bandwidth, we must determine the Y-values at points 3 dB below this peak, that is, at –10.773dB. Clicking the 8th button from the left puts the cursor into the mode in which it automatically seeks a given Y-value. Click on the Left button, then the Right button (twice if necessary) to place cursors either side of the peak (**Figure 22**). Below the graph we read off the X-value of the left cursor, which is 1.869 kHz, and the value for the right cursor, which is 2.118 kHz. The bandwidth is 2118–1869 = 249 Hz, impressively close to the required 250 Hz.

STEPPING

One of the useful features of a simulator is the ability to step or sweep component values over a given range in steps of a given size. This is so much more convenient than experimenting by desoldering and resoldering, or by plugging a series of components of a range of values into a breadboard. We use the Stepping facility to tune the filter response to exactly 2 kHz, by varying R3. In AC analysis, click on the Stepping button, which brings up the Stepping window. First of all Step What; the selector button at the right displays a list of steppable components; select R3. The box below shows what parameter(s) can be stepped, in this case only its Value. In the next 3 boxes enter the From, To, and Step Value. Try 900, 1300 and 100. Click the radio buttons for Status On, Method Linear, and Type Component, then OK. This enables stepping, in which the analysis is automatically repeated for each of the 5 steps. Reduce the Frequency Range to '2.2k, 1.8k' to obtain a closer view of the response and run the analysis (**Figure 23**). The 3rd curve (from the right) is best, centred on 2 kHz; this is the curve for R3 = 1100 Ω. Note that the peak output is unchanged because tuning has no effect on gain in this circuit. It has no effect on bandwidth either. From now on, we reduce the frequency range and the stepping range to home on a value for R3 which produces exactly 2 kHz. Soon it becomes clear that the value is somewhere between 1085 Ω and 1095 Ω. If we run without stepping, with R3 = 1085 Ω and again with R3 = 1095 Ω, we obtain peaks at 2.003 kHz and 1.994 kHz respectively. Interpolating gives the best value for R3 as 1.088 kΩ.

Temperature is another quantity that can be stepped. In the Limits window, enter the temperature as 'maximum, minimum, step'. For example '0, 100, 10' means step from 0 °C to 100 °C in steps of 10 degrees. In this circuit, such a range makes virtually no difference to output. Finally, we can step component values within their normal tolerance ranges.

ANSWERS TO INVESTIGATION (2)

Last month's investigation concerned improving the low-frequency response of an amplifier. Altering C1 or C2 makes virtually no difference, but increasing C3 has a marked effect. This stabilises the emitter voltage more strongly, preventing the low frequencies being lost to ground. The best response is with C3 = 330 µF as in **Figure 24**. The plotted Frequency Range is reduced to 10 Hz–1 kHz, the region of interest. Output at Node 6 is plotted on a decibel scale. Using Cursor mode, place the right cursor as far as possible to the right, to read the maximum output level (8.766 dB). Place the left cursor on 30 Hz, the lowest frequency to be passed. The level of this is and the Delta column shows that this is 2.919 dB below the maximum, close enough to -3 dB, and using a capacitor of standard value.

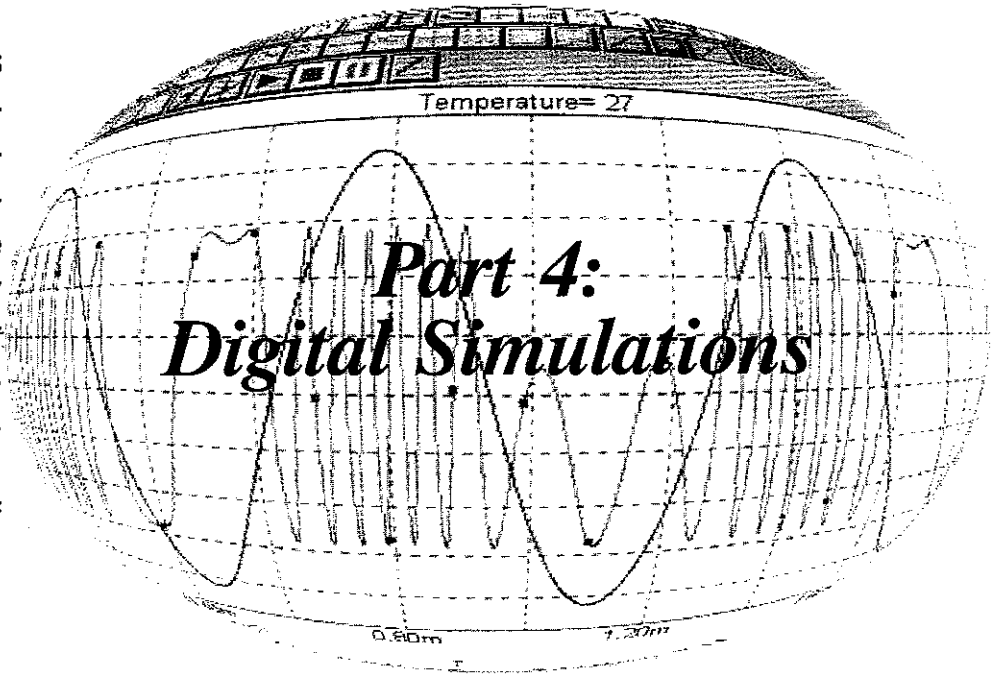
INVESTIGATION (3)

The circuit of Fig 20 is set up with these values: R1 = 3.6 kΩ, R2 = 22 kΩ, R3 = 36 Ω, R4 = 10 MΩ, C1 = C2 = 1 nF. Find the centre frequency f_c, the bandwidth, and the gain at f_c.

[960103-11]

HANDS-ON ELECTRONICS

a short course in circuit simulation



Part 4: Digital Simulations

The digital circuits supplied as demonstrations with a simulator are usually intended to impress the prospective user by their complexity. Only people used to scanning digital schematics can comprehend them. In this part of the article we will help the beginner to get the feel of digital networks.

AN EASY START

We begin with something very simple; one digital signal generator sending its one-bit signal to one logic gate (see **Figure 25**). MC5 refers to a digital signal generator as a Stimulus Generator. Several are available, with 1, 2, 3 or 4 outputs. We need a 1-bit output, so click on Components → Digital Primitives → Stimulus Generators → Stim1. The Component window lists 7 statements. The first, FORMAT, refers to the way the bits are formatted (or grouped). Here we have only one bit so the format can only be '1'. The COMMAND statement defines how the output is to vary with time. Type in these items in a single line as in **Table 1**. The loop can be run any number of times; -1 TIMES means repeat indefinitely. Timings can be in seconds or submultiples greater than nanoseconds.

The output from the generator is fed to a 2-input NAND gate (in the figure, the node number obscures the small circle denoting 'invert'). The Components window has all the default statements ready set, except for MODEL. Select D0_GATE from the list of models on the right. Connect the devices as shown, wiring the two inputs of U2 together so that it operates as an inverter.

With digital simulations we use the Transient Analysis far more than AC or

Table 1

Item	Interpretation
0 ns 0	*at time zero (0 nanoseconds) output is level 0*
LABEL = START labels a point in the sequence, named START.	*You could call it anything else, such as LOOP, BEGIN, REPEAT*
50 ns 1	*at 50 ns (from time zero) make the output 1*
100 ns 0	*at 100 ns make the output 0*
200 ns 1	*at 200 ns make the output 1*
210 ns 0	*at 210 ns make the output 0*
240 ns 1	*at 240 ns make the output 1*
260 ns GOTO START 2 TIMES	*at 260 ns go to the label start and continue from there run the loop twice.*

Spectrum Software (UK) trading as Rainbow Software have advised us that a **fully functional** version of Micro-Cap V is available to any of our readers via their Internet WEB site. The URL of the WEB is

http://www.micro-cap.co.uk

Readers will be able to instantly download the software **free of charge**.
Rainbow Software also provide a support WEB for **all** Micro-Cap users.
Readers not on the Internet can contact Rainbow Software at
Ash Lea House
Oldfield Road
Bromley, Kent BR1 2LE
Telephone 097 328 8242
Voicemail/fax 0181 295 4500
E-mail: rainbow@micro-cap.co.uk

By Owen Bishop

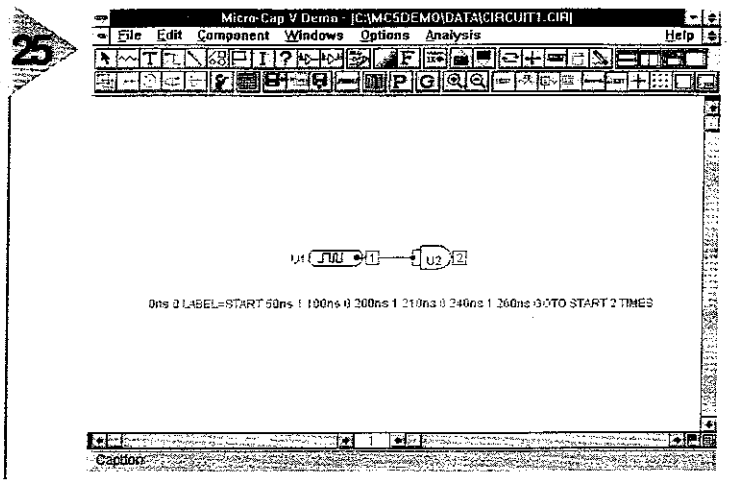


Figure 25. Simple beginnings: one digital signal generator sending a one-bit signal to one logic gate.

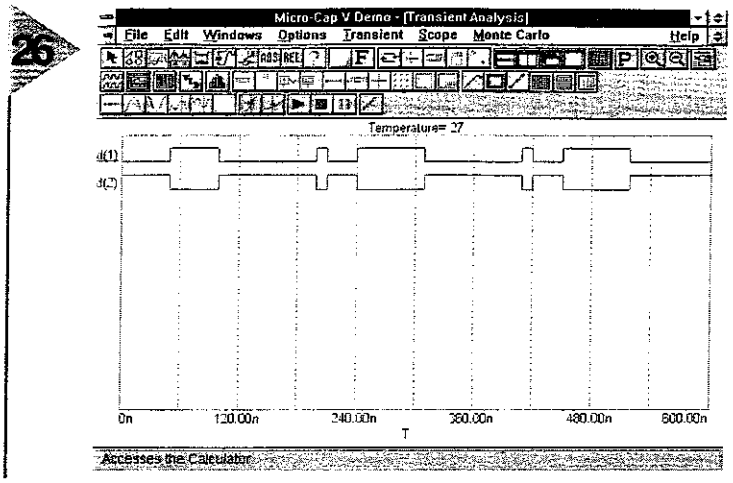


Figure 26. Waveforms resulting from the action of the setup in Figure 25.

DC. In the Transient Analysis Limits window, set the Time Range to 600 ns, to allow time to go round the loop just over twice. Check the Auto Scale Ranges box. The X Expressions are T, and the Y Expressions are D(1) and D(2) respectively (D for digital). Then Run. The result is **Figure 26.** The upper plot shows the sequence of pulses generated according to the command statement for U1. The lower shows the signal as inverted by the NAND gate.

Try working out other sequences of pulses and plotting them in a Transient Analysis. Instead of 0 and 1 for pulse level, you can use RND or ? for a randomly chosen level, R for a level rising from 0 to 1, F for a level falling from 1 to 0, X for an unknown level, and Z for the high-impedance state.

Table 2

U4	*constant high level to J, K and SET inputs of flip-flops, COMMAND = 0ns 1*
U5	*clock, generating 50ns pulses (10MHz), COMMAND = 0ns 0 LABEL=START 50ns 1 100ns 0, 150ns GOTO start -1 TIMES*
U6	*provides an initial low pulse to reset the flip-flops to 000 output, COMMAND = 0ns 0 5ns 1*

PULSE COUNTER

Now to try something more elaborate. **Figure 27** is a 3-bit counter, built from J-K bistables (flip-flops) (U1-U3). To obtain these, click on Component → Digital Primitives → Edge-Triggered Flip-Flops → JKFF. There is only the Timing Model to select, which is D0_EFF. There are three Stimulus Generators, all with FORMAT = 1 – see **Table 2.**

A Transient Analysis of this network, with Time Range of 1μs (1u), and with Auto Scale Ranges checked, gives **Figure 28.** We have asked for plots of digital levels at nodes 1, 2, 3, 4, 6, and 8. The results are:

- d(1) continuously high, as required
- d(2) shows an initial low resetting pulse, then is continuously high, as required
- d(3) the 10MHz clock
- d(4), d(6) and d(8), considered as a 3-bit binary number

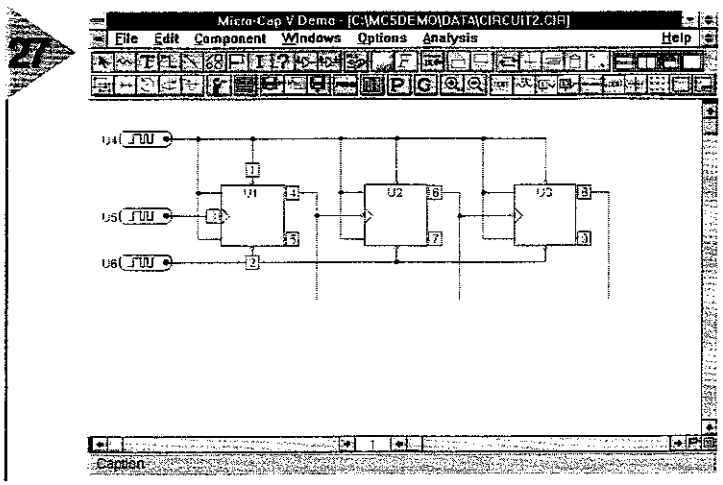
d(4) is the least significant bit incrementing from 000 to 111 repeatedly, as this is a modulo-8 counter. As an alternative, try plotting the output sequence of the inverting outputs of the flip-flops, d(5), d(7) and d(9), and note what sequence of values it produces.

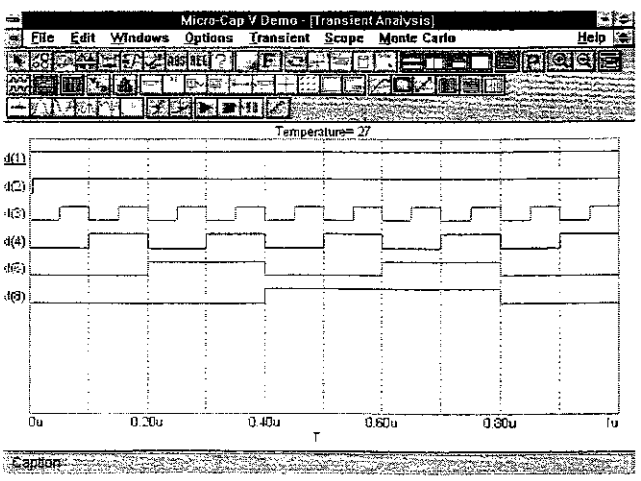
MORE LOGIC

Different states of the counter output can be detected with suitable logic. The simplest state to detect is 000, for which we need a 3-input NOR gate; its output goes high when all three inputs are low. Add such a gate to the network of Fig. 27.

Figure 27. Schematic of a 3-bit counter built from J-K bistables.

Figure 28. Waveforms resulting from the action of the circuit in Figure 27.





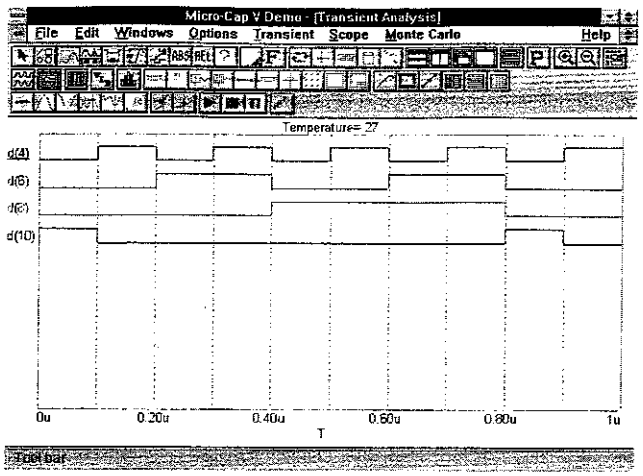


Figure 29. Waveforms resulting from adding a 3-input NOR gate to the network in Figure 27.

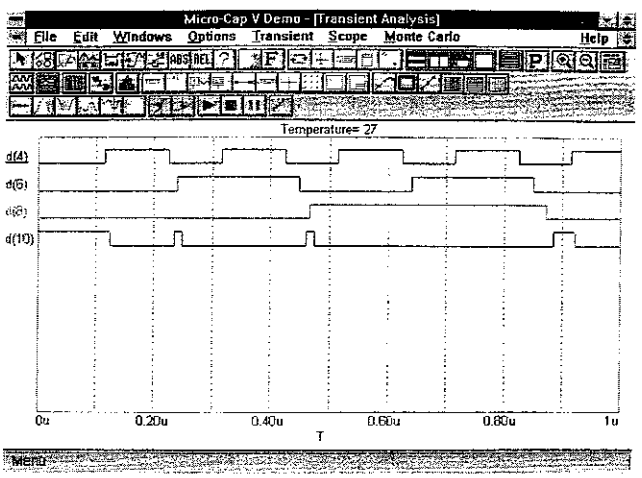


Figure 30. Waveforms as in Figure 29 but with delay times added to the network.

For its Timing Model, select D0_GATE. Plot its Transient Analysis. As **Figure 29** confirms, the output of the NOR gate d(10) is high whenever the bistable outputs are all low. A network of this type could be used, for example, to flash an LED whenever the count is 000. Typically, the circuit would be operating at a frequency much lower than 10 MHz. The clock rate might be 2 Hz, producing flashes 0.5 s long at each count of 0. Or the clock pulses might be generated irregularly, perhaps by objects passing on a conveyor belt. But in applications in which a high clock rate is required, there is a hazard that needs investigation. This is the effect of delays within the logic elements. We have modelled the circuits with zero delay (D0_EFF and D0_GATE) with the result that Figures 28 and 29 are neatly in accordance with the truth tables. A real bistable or gate does not change state instantly. After the inputs have changed there is a delay before the output changes. For instance, the typical propagation delay of a TTL gate is 11 ns, which is of the same order as the pulses in a 10 MHz network. We can simulate these delays by changing the Timing Models. Use the select arrow to click on each element in turn and edit its Component window. For the flip-flops, change the Timing Model to DLY_EFF. Change the NOR gate model to DLY_TTL. Rerun the analysis (**Figure 30**) and note how, when the output of one counter goes low there is a delay before the output of the next counter changes state. This is why a counter such as this is known as a ripple counter.

Note the glitches on the plot of d(10). As the count changes from 001 to 010 [remember, d(4) is the least significant bit], d(5) does not go high until several nanoseconds after d(4) has gone low. There is a transient state in which all outputs are low (000). This is detected by the NOR gate and a short high pulse is generated. The next time this occurs is in the transition from 011 to 100, which actually goes through two transition stages, 010 and 000. The second of these causes another glitch. Eventually the count changes from 111 to 000 (extreme right of plot) and here there are two transition stages, 110 and 100, which delays the start of the high pulse on d(10), making it less than half the length than in Fig 29. It could happen in a counter with more than 3 bits that the delays at each stage would allow d(4) to go high again before the other outputs have all gone low, so there would be no high pulse on d(10) at this stage. The circuit would skip a count. **Figure 30** demonstrates one of the most serious problems in the design of high-speed logic circuits, and emphasises the importance of using circuit simulators. These glitches appear on slow-speed circuits too but, if

Table 3

U5	a 500Hz clock, COMMAND = 0ms 0 LABEL=START 1ms 1 2ms 0 3ms GOTO START -1 TIMES
U6	holds set and reset inputs high, COMMAND = 0ms 1

Figure 31. Schematic of a so-called walking-ring counter.

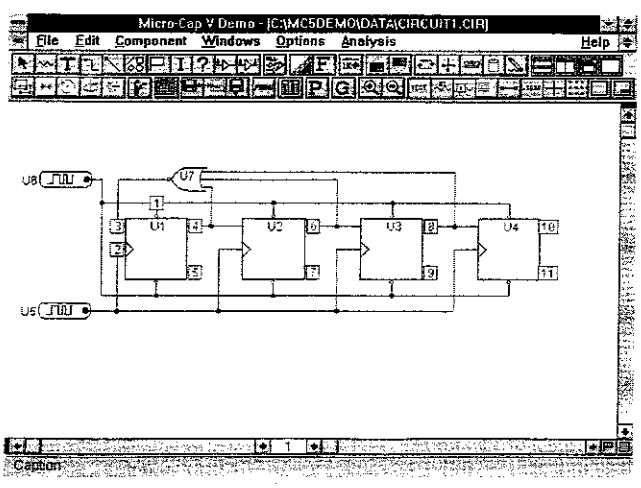
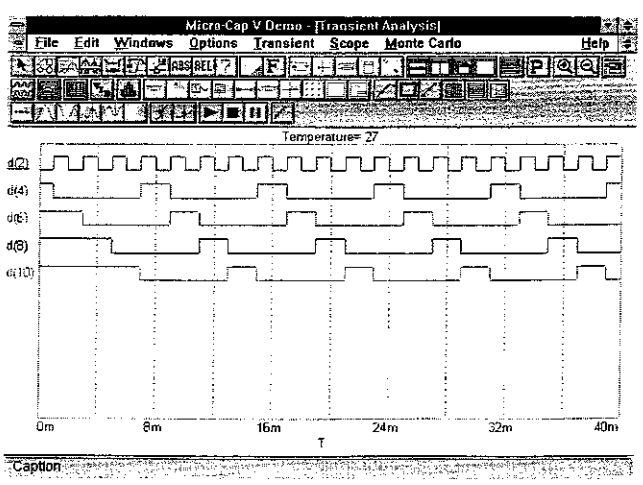


Figure 32. Output signals of the walking-ring counter.



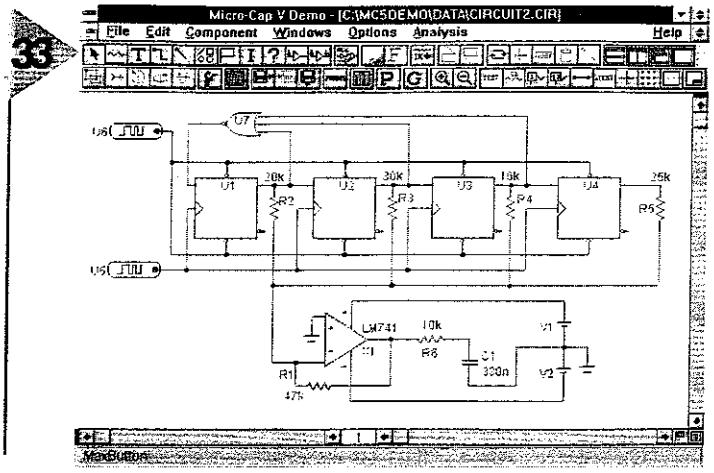


Figure 33. Schematic of Figure 31 modified by weighting the bistables by linking them to a summer.

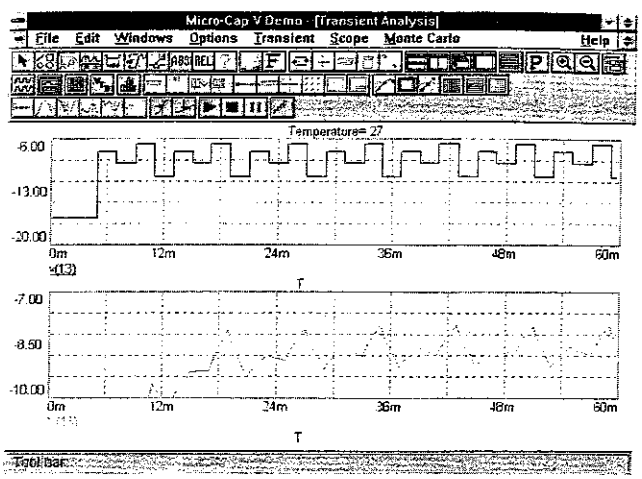


Figure 34. Waveform resulting from a 60 ms Transient Analysis of the output of the op amp in Figure 33.

the circuit is driving an LED or a relay, the glitch is too short to be noticed and it is safe to model the circuit with a no-delay timing model. At high speeds, propagation delays must be taken into account. For high-speed applications, a circuit such as this counter needs to be re-designed, or replaced by a synchronous counter.

MIXED MODE

Some simulators handle only analogue circuits, while others are specialized to simulate only digital circuits. MC5 and several other advanced simulators are able to simulate circuits comprising both analogue and digital sections. This is known as mixed mode simulation. As an example of this, we simulate a digital circuit which generates an analogue waveform. The digital section consists of a walking-ring counter (**Figure 31**), a counter which has a series of outputs which go high one at a time, in a repeating sequence. The counter is built from four D-type bistables. A counter with more stages could produce a more precisely-defined waveform and, as an exercise in digital simulation, the reader can extend the example given here to 8 bits or maybe 12 bits.

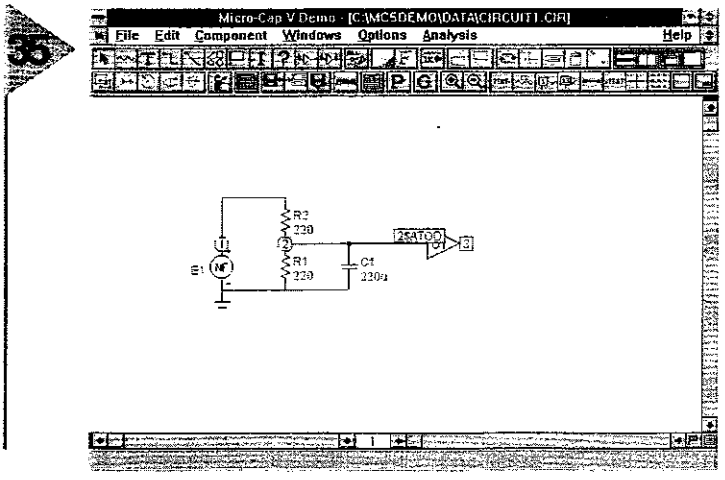
Select D0_EFF as the Timing Model for the edge-triggered bistables (DFF). There are two 1-bit Stimulus Generators (Stim1), all with FORMAT = 1 (see **Table 3**).

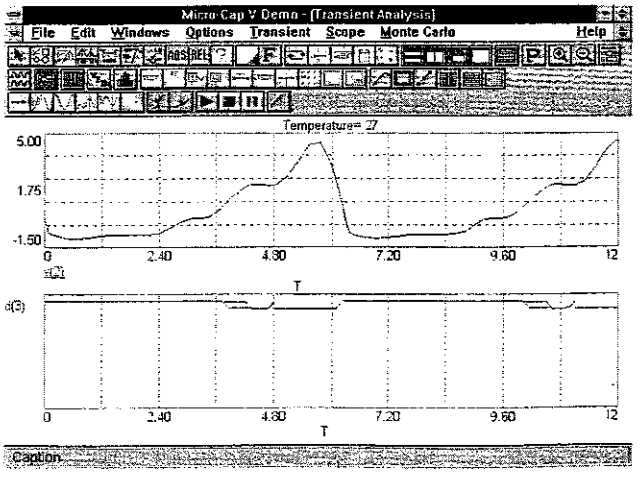
The 3-input NOR gate, U7, has D0_GATE as its timing model. Test the counter before proceeding. If each bistable is set to begin with, the feedback from the NOR gate causes the output to change in the first three counts from all 1s to a single 1, which then circulates around the counter indefinitely. We could use an initial low pulse to set the counters, but there is another way of doing this. This is to set the Global Parameter DIGINTISTATE to 1. Find this by clicking on Options Global Settings. DIGINTISTATE can be set to 0 or 1, so that all latches or bistables are reset or set to begin with, or to 2 which sets or resets them at random. The result of a 40 ms Transient Analysis is shown in Fig. 32 in which d(2) is the clock. All outputs are high to start with, but they go low in turn until only one output is high at any one instant, as expected in a ring counter. This completes the digital section of the circuit.

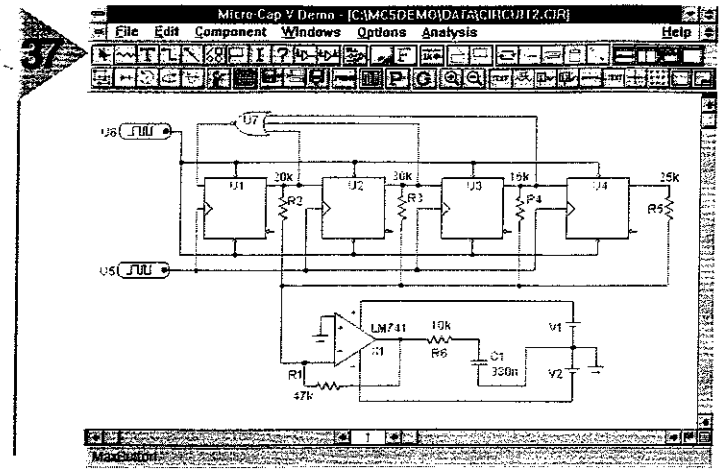
The next step is to use these outputs to feed currents of different values to the input of an op amp summer. In **Figure 33** the outputs from the bistables are weighted by connecting them to the summer through resistors of different values. We have used LM741 as the op amp model, but almost any other one will do. V1 and V2 are set to 18 V each to power the op amp. Figure 33 is displayed without node numbers to allow the connections to be clearly seen. If node numbers are enabled, we find that the nodes at which the digital section connects to the analogue section have had digital-to-analogue converters added to them. These are not converters in the usual sense (though it is possible to simulate various kinds of converters when required) but are interfaces between the two sections,

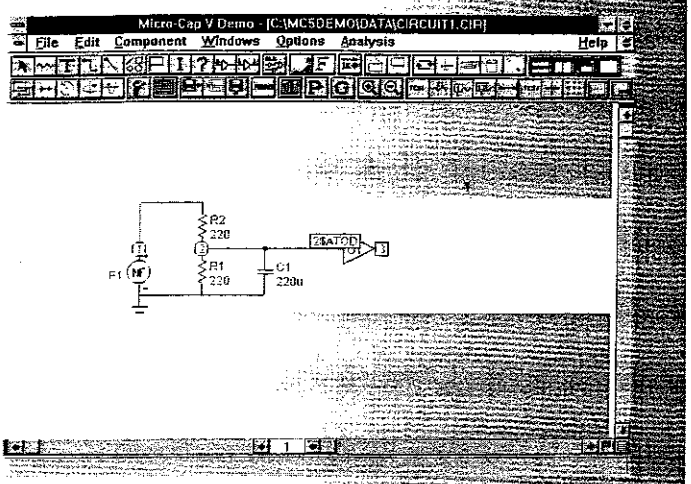
Figure 35. Use of a potential divider to release a signal which is smoothed at the same time by a capacitor.

Figure 36. This digital signal is not satisfactory because its transitions are not clearly defined.









automatically placed there for the benefit of MC5 in performing its analyses.

Figure 34 shows a 60 ms Transient Analysis of the output from the op amp V(13). This has a stepped form as each output from the counter goes high in turn. Although this is an analogue waveform, it reveals its digital origin. The signal is passed through a low-pass filter to node 16, where it has the appearance of a modified triangular wave. When plotting these curves we selected Auto Scale Ranges for the first few trial runs. The curve for V(13) fitted neatly in the automatically selected ranges (0.06, 0 and –6, –20). But the curve for V(12) begins with very low values when most of the outputs are '1', which means that the interesting part of the curve is plotted with too small an amplitude to show the waveform clearly. So we deselect Auto Scale Ranges. We leave the ranges unchanged for V(13) but edit those for V(12) to 0.06, 0 and –7, –10.

This circuit is a simplified version of a function generator IC. By increasing the number of stages and by choosing resistor values carefully, it is possible to approximate to many kinds of waveform, including sine waves. Here is a field for experimentation by the reader.

MORE MIXED MODE

In this circuit we pass a signal in the reverse direction, from an analogue circuit to a digital circuit. This is also a chance to look at the formula-type voltage source, or NFV, which is one of MC5s Function Sources. When this is placed, the Component window asks for its VALUE, which is a formula expressing the output voltage in terms of other voltages or currents and of time. In this example, enter:

VALUE = 3*PI – 6*sin(t)
– 3*sin(2*t) - 2*sin(3*t)
– 1.5*sin(4*t)

where PI is π, equal to 3.1416 and * signifies multiplication. If you have read about Fourier series you may recognise that these are the first 5 terms of the series which defines a saw-tooth waveform. The amplitude of this waveform is just over 9 V and its frequency is 0.159 Hz. If you try to connect the NFV directly to a logic gate, you will get a 'Digital Warning' from MC5 that the voltage is too high, assuming that the logic operates on 5 V. Use a potential divider to reduce this (**Figure 35**), add a capacitor to smooth the waveform, and feed the signal to a digital inverter gate. MC5 automatically puts an A-to-D converter in place. The Transient Analysis (12 s, 501 points) shows the voltage waveform at node 2 and the digital output at node 3 (remember that this is for MC5's use and does not form part of a real circuit). The digital output (**Figure 36**) is unsatisfactory because, although it is low when V(2) is high, and high when V(2) is low, as might be expected from an inverter, there are occasions when V(2) is slowly changing between high and low and the output of the inverter is indeterminate. At 4.8 s when there is a small local fall in V(2), there is a momentary high spike on the output.

This is a common problem when analogue and digital circuits are connected. To improve the interface between them we must make sure that V(2) never lingers around the threshold input level of the inverter. One way to do this is to insert an op amp, wired as a comparator between the source and the potential divider (**Figure 37**). The battery V3 provides a reference level, or this could be provided by a voltage reference or a variable potential divider in a real circuit. The plot (**Figure 38**) shows the original waveform, and that of the op amp output, after being reduced by the potential divider (multiplied by 4 in the display to make its shape easier to see). Note that although it is a squarish wave, it is still an analogue one. Its transitions are so much sharper than those of the original waveform that the output of the inverter d(4) now switches between high and low with only a very short indeterminate state, just about discernible as a thickening of the trace on the changes of state.

Once you can get an analogue circuit to change the state of a logic gate, you can get it to do almost anything. As an MC5 exercise, build logical circuits on to the inverter gate to, for example, trigger a bistable or a counter. You could add another interface between the analogue and logical sides to trigger the bistable to reset as the analogue voltage falls below a given level. Or use the output from the inverter to enable or disable a pulse train from a Stimulus generator. Such a circuit could be used to flash an LED when the analogue level exceeds a given value, and could be the basis of a frost warning or over-heating device.

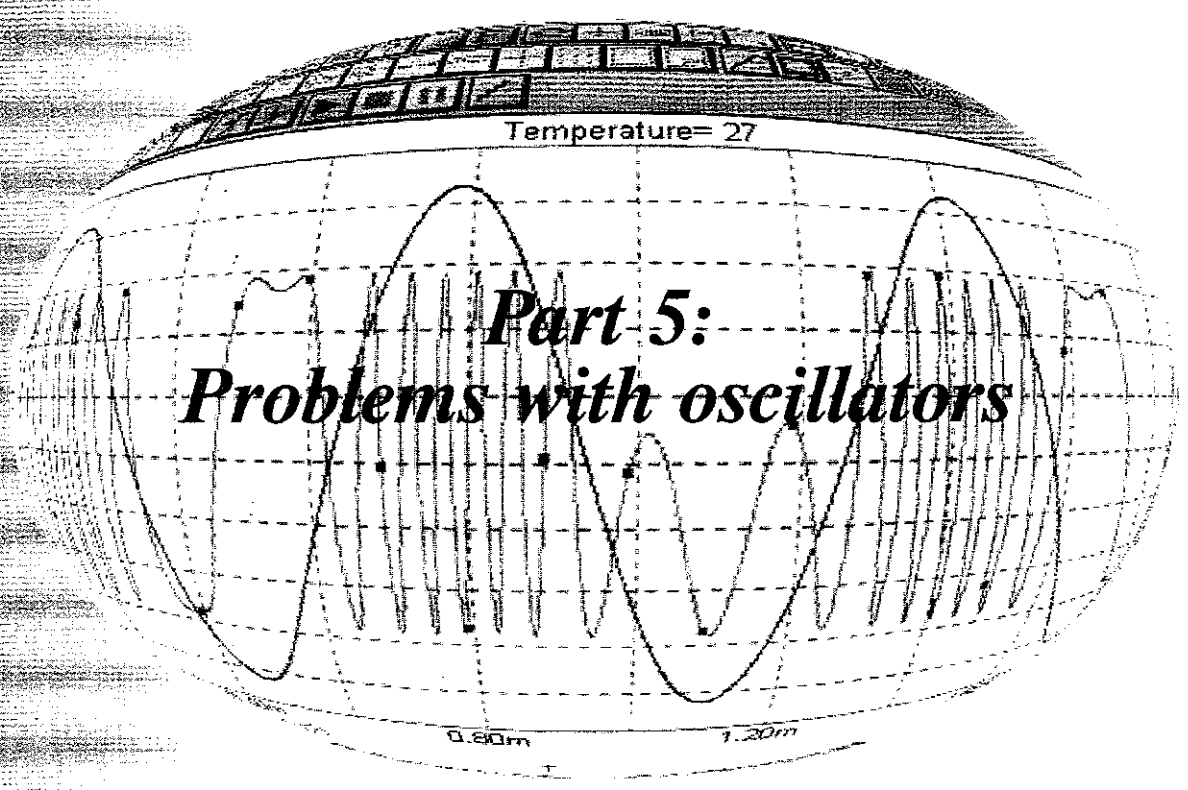
ANSWERS TO INVESTIGATION (3)

The filter presented for investigation last month is first examined by an AC analysis, with the frequency range from 100 Hz to 1 MHz. This shows a clear peak at 123 kHz. Closer examination over the range 100 kHz to 150 kHz gives f_c = 123.500 kHz. On the same graph we find the –3dB points at 120.960 kHz and 126.127 kHz, a bandwidth of 5.167 kHz – a narrow band filter. A Transient analysis with the frequency of V1 set to 123.5 kHz shows that amplitude comes to a steady value after about 80 μs and, given input amplitude 0.1 V, the output amplitude is 0.21 V, a gain of 2.1.

(960024-4)

HANDS-ON ELECTRONICS

a short course in circuit simulation



Part 5: Problems with oscillators

The fifth and final part of this short course investigates problems that may be encountered with all kinds of oscillator and shows how to analyse such problems.

By Owen Bishop

The first circuit chosen for this month's investigations is a relaxation oscillator based on an n-p-n BJT and a p-n-p BJT (**Figure 39**). It can be used for purposes ranging from flashing an LED to producing an audio-frequency signal. The rate of oscillation depends on the value of C_1 and the ratio of R_1 to R_2. Assemble the circuit, choosing the pair of transistor models shown, or use other models from the selection box on the right of the Components window. Select Analysis → Transient Analysis then, in the Transient Analysis Limits window, enter Time Range 0.3s, Maximum Time Step 1m, and select Auto Scale Ranges. Set up the plot details boxes to plot curves, for V(1), V(2) and V(5)-V(1) (the pd across C_1) against time T.

Running the analysis produces a disappointment. Instead of three interesting waveforms, we have three horizontal lines across the screen. V(1) is constant at 4.1 V, V(2) is constant at 0.9V, and V(5)-V(1) is constant at 4.2 V. The oscillator is not oscillating. Click on the Numeric Output button to find out why. The Numeric Output screen shows the results of the DC Operating Point analysis, which is undertaken automatically before a Transient Analysis. It produces a set of node voltages and branch currents to act as a starting point for the Transient Analysis. The Numeric Output shows that the node voltages are:

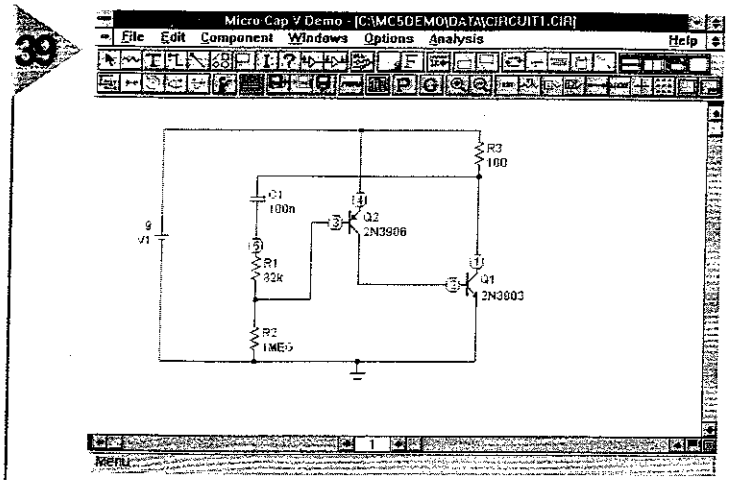
V(1) = 4.14V V(2) = 0.882V
V(3) = 8.33V V(4) = 9V
V(5) = 8.33

There is zero pd across C_1, a sure sign that nothing is happening or will happen. The window also tells us about the operating conditions for the transistors, including the facts that:

For Q1 (npn): vBE = 0.0882V and iC = 4.9mA
For Q2 (pnp): vBE = -0.669V and iC = 0.9mA

The voltage levels in the circuit are such that it is almost ready to oscillate, but not quite.

Situations such as this often arise when SPICE analyses oscillator circuits, particularly those of relaxation oscillators. It may also occur in circuits with



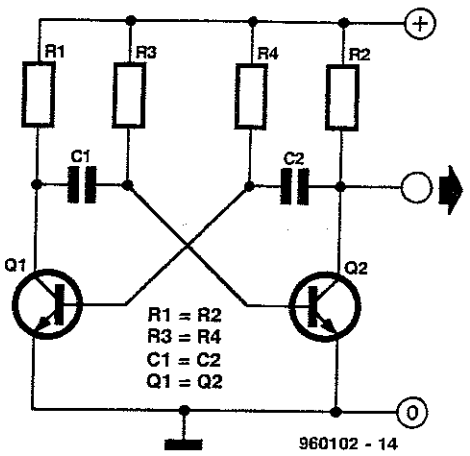


Figure 39. Relaxation oscillator based on an n-p-n BJT and p-n-p BJT.

Figure 40. Basic circuit of astable oscillator.

various kinds of feedback. The Operating Point analysis takes the circuit to a stable state, maybe a rather uncertain one but nevertheless stable, so that the Transient Analysis never starts oscillating. Such a state may not occur in a real circuit because slight leakages or variations of current, perhaps resulting from component heating, which are not allowed for in the models used in the analysis, would eventually produce voltages that would cause oscillations to begin. On the other hand, this circuit might genuinely be a non-starter.

SYMMETRY

A similar latch-up occurs in the astable circuit of **Figure 40.** Here the paired resistors, capacitors and transistors are identical and the Operating Point Analysis produces symmetrical voltages and currents. It goes into a stable state, and oscillation never begins. In a real circuit there are always slight differences between nominally identical components, and the asymmetry of the voltages and currents is sufficient to ensure that the circuit goes straight to one of its two astable states and, from there, oscillation begins. One solution to this problem is to deliberately introduce asymmetry. An obvious technique is to make one of the resistors larger than its symmetrically opposite one. The reader might assemble this astable and try to get it started by modifying one of the component values. It is not always easy to find a value that will bring about oscillation.

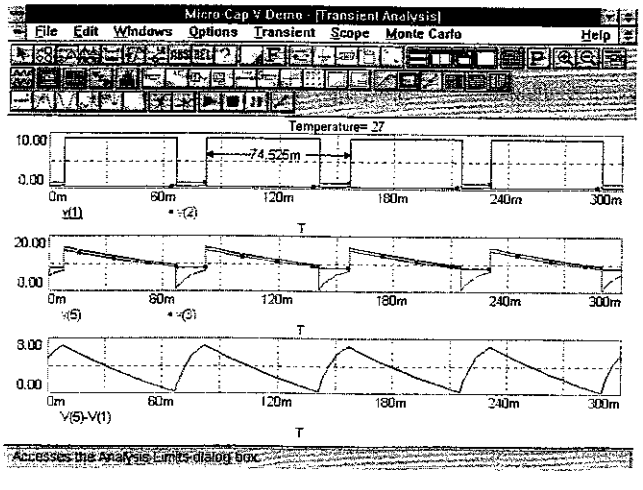
INITIAL CONDITIONS

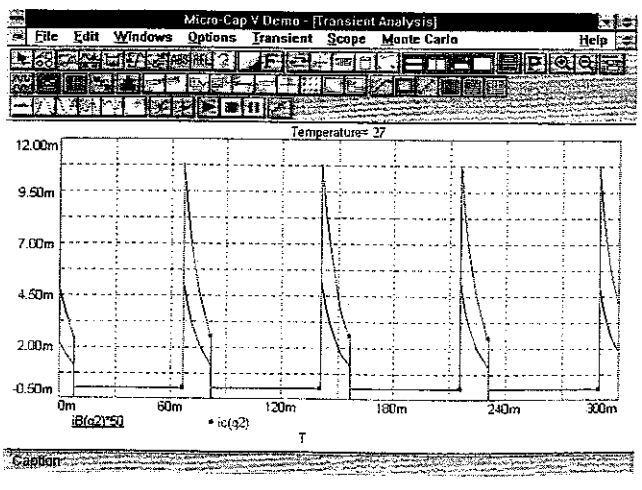
Altering resistor values in Figure 39 might induce that oscillator to start more readily, and this is left as an exercise for the reader. The main drawback of this technique is that one of the resistor or other values has been made incorrect, which may affect the frequency, the mark-space ratio or other characteristics. Fortunately, SPICE provides another way of ensuring that the circuit starts oscillating. This is done by stipulating certain initial conditions to take effect before the Transient Analysis begins. By reasoning or (sometimes) guesswork, we set one or more node voltages to values that we think will set the circuit oscillating. In this circuit, it might help to turn Q_2 fully on. Do this by bringing its base voltage (node 3) lower than the quiescent 8.33 V. If we make it 7 V, Q_2 is turned fully on, causing a full collector current to flow through Q_2, to become the base current of Q_1 and turn that transistor fully on too.

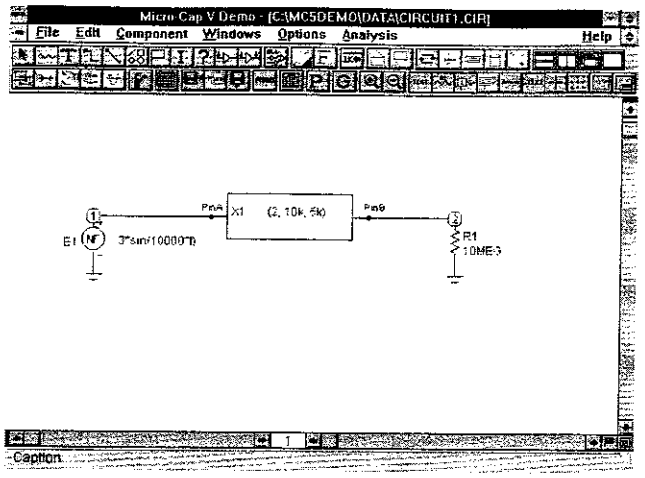
Initial conditions are set by using the .IC command. Exit the analysis, then display the Text window by clicking on the small square at the bottom right corner of the Schematic window. There you will see the model statements for the transistors.

Figure 41. Set of graphs showing how the astable oscillator in Figure 39 works.

Figure 42. Plot of the base and collector currents of Q_2 in Figure 39.







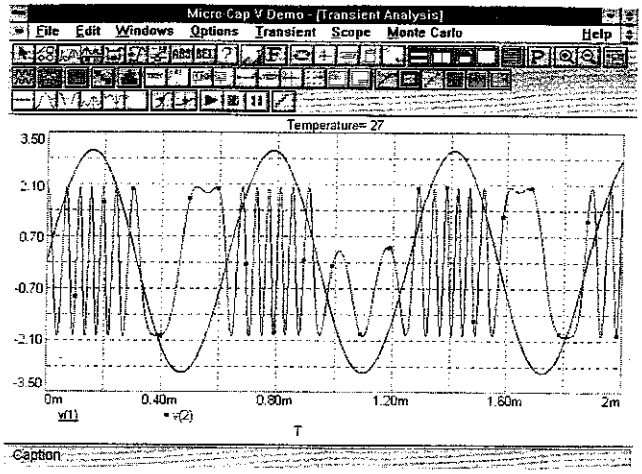


Figure 43. Basic circuit for illustrating how a macro can be inserted.

Figure 44. Showing the effect of the output of E1 on the output frequency of X1 in Figure 43.

Below these type:

.IC V(3) = 7

When the analysis is called, the voltage at node 3 is set to 7 V for the Operating Point and the voltages at other nodes calculated accordingly. To find out what difference this makes, go to the Transient Analysis Limits window and check the Operating Point Only box, then Run. Clicking on the Numeric Output button produces the operating point analysis, but now with different results:

V(1) = 2.07V V(2) = 2.89V
V(3) = 7.00V V(4) = 9V
V(5) = 7.00V

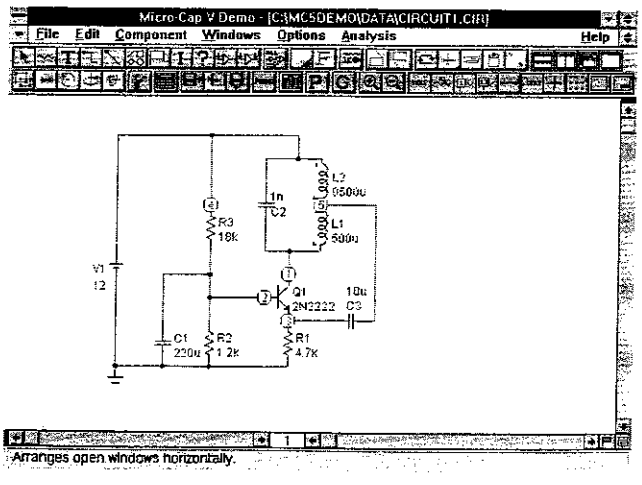
Q_2 is clearly fully on, as can be confirmed by its vBE, which is 2 V and its collector current, which is 1.27 A. This introduces a note of caution, for this is a large current, more than a 2N3906 is rated for. This illustrates how much safer it is to work with a simulator. Applying 7 V to a real circuit to kick it into action could well burn out both transistors instantly. But we shall need to check that such large currents never occur when the circuit is oscillating normally.

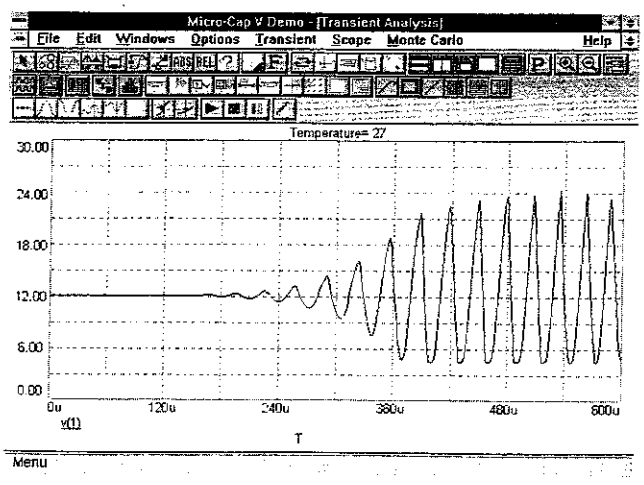
To see if we have managed to get the circuit oscillating, go to the Transient Analysis Limits window, deselect the Operating Conditions Only box, then Run. The result clearly shows that the oscillator is running. The most useful set of curves for understanding how the oscillator works is plotted in three graphs (**Figure 41**), all against time (*T*). To make the plots distinguishable when printed in black, we have clicked on the Tokens button (middle row, 4th from right). Graph 1 shows V(1) and V(2), from which it can be deduced that Q_1 and Q_2 are both OFF at the same time, that is when V(1) is high and V(2) is slightly raised owing to current flowing from Q_2 to Q_1. When Q_1 turns OFF, there is a sharp rise in V(1), which leads to V(5) being pulled sharply up (to 16 V). R_1 and R_2 act as a potential divider, so V(3) is pulled up sharply too, and Q_2 is turned off. This cuts off the base current to Q_1, keeping it turned OFF. This is one of the stable states. Then V(5) gradually falls as charge leaks away through R_1 and R_2 to ground. Eventually V(5) and V(3) fall to a level at which Q_2 turns on again. It supplies base current to Q_1, turning it on. Q_1 and Q_2 are both ON at the same time, which is the other stable state. Turning Q_1 ON reduces V(1) sharply, pulling down V(5). But V(3) remains at about 8.4 (one diode drop below 9 V), so C_1 is gradually charged again. Eventually V(3) rises above 8.4 V, turning off Q_2, and thus turning off Q_1. The cycle is complete. Using the Horizontal measure mode on Graph 1 allows the period of the oscillation to be determined as 74.525 ms, or 13.4 Hz. The third graph in Figure 41 shows the changes in pd across C_1 as it is alternately charged and discharged, the waveform clearly showing the exponential rise and fall of pd.

Figure 41 demonstrates how useful a simulator can be when trying to discover how a circuit operates. We can also use it to investigate whether volt-

Figure 45. Circuit diagram of typical Hartley oscillator.

Figure 46. Showing how the Hartley oscillator reaches its peak output.





ages and currents are always at safe levels. There is a query about the large current through Q_2; does this ever reach such high levels in normal oscillation? To answer this question, repeat the analysis, plotting iB(Q2) and iC(Q2) which are respectively the base and collector currents of Q_2 (**Figure 42**). The graphs show that the collector current peaks at 10.75 mA, which is well within the rating for a 2N3906. On the original plots the base current was too small for measurement but plotting iB(Q2)*50 magnifies the scale, and we can now read that the maximum base current is about 0.1 mA. Similar plots can be used to check other circuit variables. For example, plotting i(R3)*(V(1)-V(4)) shows how power dissipation in the load resistor (R_3) varies during the cycle. Carry out this check to see what maximum power dissipation must be allowed for in the load circuit, here represented by R_3.

PULSE SOURCE

Use this to instantly increase the power supply to the oscillator from 0 V to 9 V. This checks whether the oscillator will actually oscillate when switched on, without the use of the 7 V initial kick. With the Select cursor, click on the battery V1, then press the Delete key to remove it from the circuit. From the Component menu select Pulse Source and position this in the gap left by the battery. From the box on the right, select the PULSE model. In the text area you will now find its uncompleted model statement:

.MODEL PULSE PUL( )

First of all delete the .IC statement on the line above to remove the initial kick, then enter these parameters in the brackets in the pulse model:

VZERO=0	VONE=9
P1=100m	P2=100m
P3=300m	P4=300m
P5=300m	

The Help screen gives the meaning of the parameters under 'Pulse source'. The result is that the oscillator is switched on after a 100 ms delay. Plot the transient to see if the oscillator really does start when powered up in the normal way. The fact that the capacitor begins with zero charge causes an initial flow of current which makes oscillation begin.

MACROS

In Part 3 we saw how a device such as an op amp can be modelled from SPICE primitives (resistors, capacitors, transistors etc) by defining a subcircuit. The subcircuit needs to be defined only once, but it may be referred to by name in the netlist as many times as it is needed. Subcircuits are part of SPICE and, when defined, all subcircuits operate according to the same parameters. If we need similar subcircuits operating with different parameters, we must define each as a subcircuit with its own name and parameter set. The concept of a macro is similar, though not included in SPICE. The netlist of a macro is defined once and for all, after which we define its parameters every time we use it. In this sense, the macro is more like one of the primitives, such as a resistor. Every time we place a resistor on a schematic we state its resistance and optionally its temperature coefficient. We do the same for macros. Macros, like subcircuits, are built from several or even many primitives and MC5 provides a useful range of them, also referring to them as Analog Behavioral Building Blocks. Some of these, such as the amplifier AMP and the voltage controlled oscillator VCO, are applicable to most analogue circuits. Others such as DIV, which produces the result of dividing one analogue signal by another, or SLIP, which models hysteresis, are more appropriate to models of systems. The exact way that their functions are realised in terms of electronic components is left unstated. This is a black-box approach to modelling systems.

As an example of a macro we will look at VCO, which is in line with the oscillator circuit theme for this month. You can examine its structure by clicking on File → Open → VCO.CIR. The VCO consists of a voltage controlled source, input at PinA, the output of which appears across resistor. The capacitor acts as an integrator and a voltage controlled voltage source produces at its output PinB a cosine wave modified in frequency according to the pd across the capacitor. There are three parameters: the amplitude of the output signal in volts vp, the centre frequency in hertz f_0, and the frequency sensitivity in hertz per volt, k_f. To include this macro in a circuit (**Figure 43**), click on Component → Analog Primitives → Macros → VCO. After you place the VCO, the Component window asks for VALUE. The first item, VCO is already entered. After this type (2, 10K, 5K). These are the parameters defining amplitude 2 V, centre frequency 10 kHz and frequency sensitivity 5 kHz/V.

E1 is a Function Source, type NFV. After placing this, key in its VALUE, 3*sin(10000*t). This produces a sine wave, amplitude 3 V, frequency $10000/2\pi$ = 1592 Hz, for frequency-modulating the output of the VCO. R_1 is a load resistor.

To see the VCO output, run a Transient Analysis. The settings are: Time Range = 2 m, Maximum Time Step = 1 u (to obtain smoother curves), Auto Scale Ranges box checked. Plot V(1) and V(2) against time. The result is **Figure 44** in which we can see V(1) the sinusoidal output of E1 and the effect it has on the frequency of the output V(2) from X1. Experiment by varying the frequency and amplitude of the modulating signal and by varying the parameters of the VCO.

HARTLEY OSCILLATOR

This is one of the traditional capacitor-inductor oscillators, which generates a sine wave. It is based on a capacitor-inductor resonant network (**Figure 45**) which is tapped to provide feedback and maintain the circuit in oscillation. The base voltage is held fairly steady by C_1. The feedback through C_3 to the emitter affects the base-emitter voltage. This circuit requires a kick to start it (usually provided when the power supply is turned on). This is because the circuit relies on feedback through C_3 from the resonating network, a dynamic process, which is not provided in the quiescent Operating Point Analysis. Here we start it by specifying

.IC V(2)=5

This turns the transistor fully on, causing a large pd across the resonant loop, which starts the loop resonating. Output is taken from the collector, node 1. In the Transient Analysis Limits window set Time Range to 0.6 m and Maximum Time Step to 1 u. Running produces **Figure 46** in which we can see the sinusoidal oscillations gradually building up to maximum amplitude. Usually the output from this oscillator is taken from a coil wound on the same core as L_1/L_2. In a real circuit L_1/L_2 would be a single coil tapped part of the way along its length.

It is interesting to investigate the circuit, particularly by changing the value of C_2 and the values of L_1/L_2. The effect of varying the feedback capacitor C_3 is somewhat unpredictable because, if large, it may load the loop and alter its resonant frequency. If small, it may provide insufficient feedback for sustained oscillation. Find out if this circuit begins to oscillate when switched on, without needing a kick. Investigations of this circuit are left to the reader as hands-on experience in using MC5.

(960072-V)