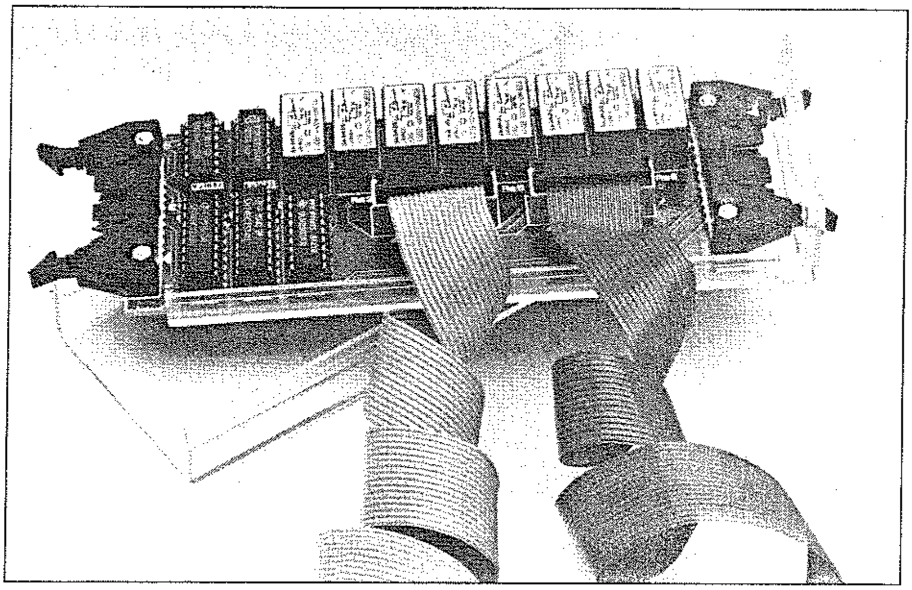
RELAY CARD FOR UNIVERSAL I/O INTERFACE



This relay card connects to the universal I/0 interface for IBM PCs described in the May 1991 issue. Simple to build and program, it offers a safe and easy way of controlling all sorts of equipment by means of a PC.

by A. Rigby

ALTHOUGH the relay card described here is designed specifically as an extension for the PC I/O interface (Ref. 1), its input control signals are readily found, or made, in non-IBM (PC) computers.

The circuit diagram of the relay card, Fig. 1, shows that it is linked to the I/O card via connector K1. It is also seen that the I/O card signals are buffered and fed to connector K4, which allows up to four extension circuits to be connected in series. Only two signals 'change' between K1 and K4: address lines A0 and A1 are interchanged on K4 (with respect to K1), and A0 is inverted. This allows all extension cards connected to the PC I/O interface to make use of a single, simple, address decoder. All cards connected in this way respond internally to address 00 (binary), but the successive interchanging of A0 and A1 causes their actual address to be determined by the order in which they are connected. Table 1 shows the address assignments.

More relays than ICs

The data flow between the PC I/O card and the relay extension is controlled by a bidirectional buffer, IC2. Although a unidirectional buffer would have been in order for the relay card (which functions as a write-only extension), bidirectional buffering is applied because two-way data flow may be required by other cards in the system.

Table 1. Address overview

Address	Relay card
base address + 0	1
base address + 1	2
base address + 2	3
base address + 3	4

The actual relay interface starts at register IC4, which is used to latch data when the relay card is addressed. The addressing is accomplished via the $\overline{ENABLE}$ and $\overline{WR}$ lines. When both are low, the output of IC1b is low also. To ensure that the data are stable at the input of the register, they are latched when the output of IC1b reverts to logic high. The logic pattern stored in IC4 is fed to driver IC5, which controls the relay coils. The relays are actuated by a logic high data bit written to IC4, so data inverting is not required.

The relay contacts are brought out to pins on connectors K2 and K3. Connector K2 carries the mother contacts and the normally open (NO) contacts of the relays, and K3 the mother contacts and the normally closed (NC) contacts.

Table 2. Relay specifications

Siemens V23040-A0001-B201
Contact specifications

Max. switching voltage:	150 V d.c. 125 V a.c.
Max. switching current:	2 A
Max. continuous current:	2 A
Max. switching power:	35 W d.c. 60 W a.c.
Max. switching frequency:	100 Hz
Mechanical lifetime:	10^8 s.o.
Mechanical lifetime with contacts loaded:	10^3 - 10^8 s.o.

s.o. = switching operations

Building and testing

The relay extension is built on a double-sided, through-plated printed circuit board, of which the track layouts and the component overlay are given in Fig. 2. The construction is mostly straightforward soldering work. The completed card is connected to the PC I/O interface via a 20-way flatcable with IDC connectors at both ends.

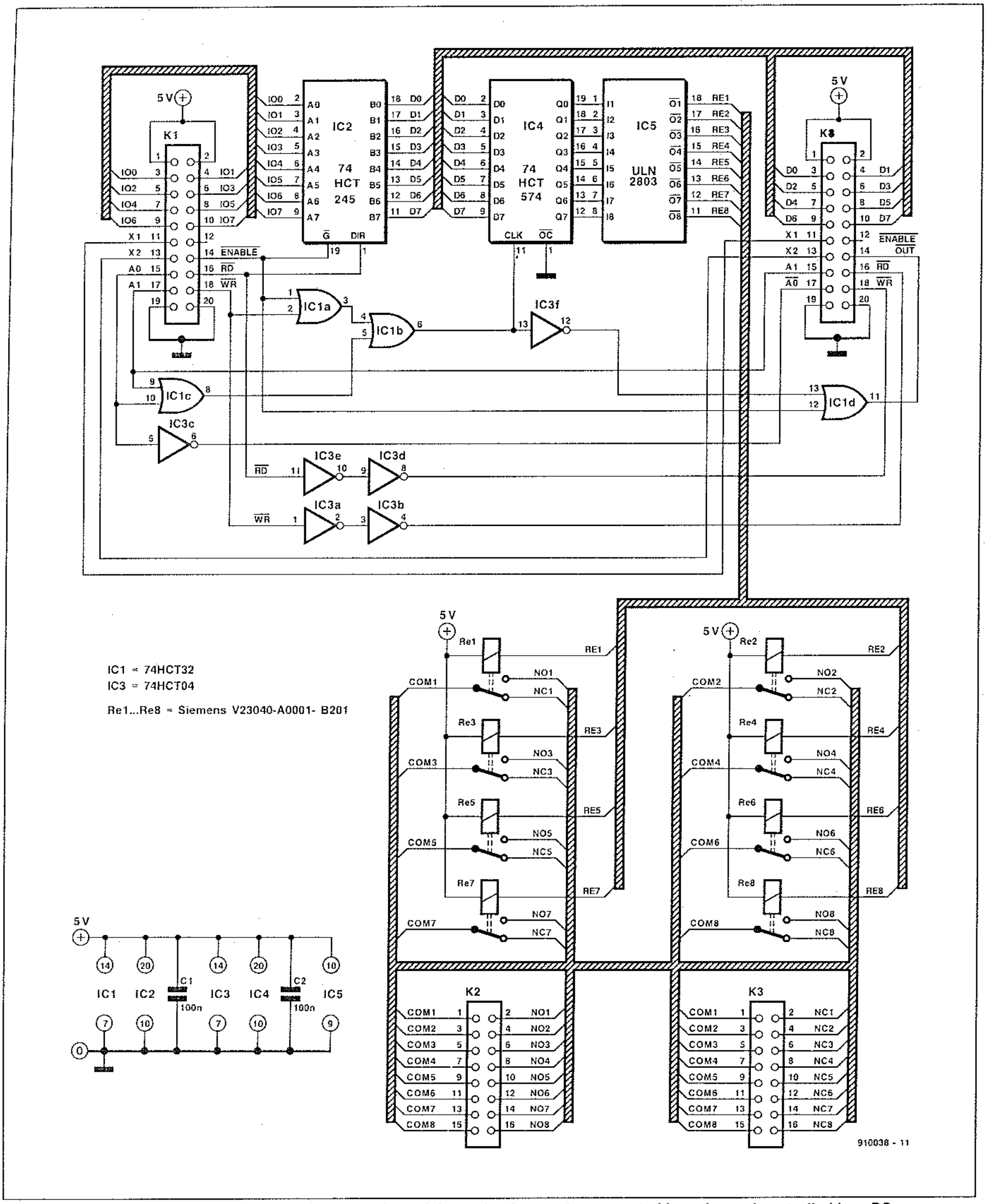


Fig. 1. Circuit diagram of the relay extension. Up to four of these circuits may be connected in series and controlled by a PC.

The current consumption of the relay card is determined by the number of actuated relays. When all relays are actuated, the current consumption is a little below 150 mA.

The switching functions of the relay card may be tested with the aid of the program listed in Fig. 3. When run, this program causes the relays to be actuated and deactuated in succession. The program may be used to test up to four relay cards connected in series.

Because of the track layout of the printed circuit board, the maximum voltage that may be switched by the relays is 42 V a.c. or 60 V d.c. This means that the relay card may **not** be used to switch mains loads directly.■

Reference:

1. Universal I/O card for IBM PCs. *Elektor Electronics* May 1991.

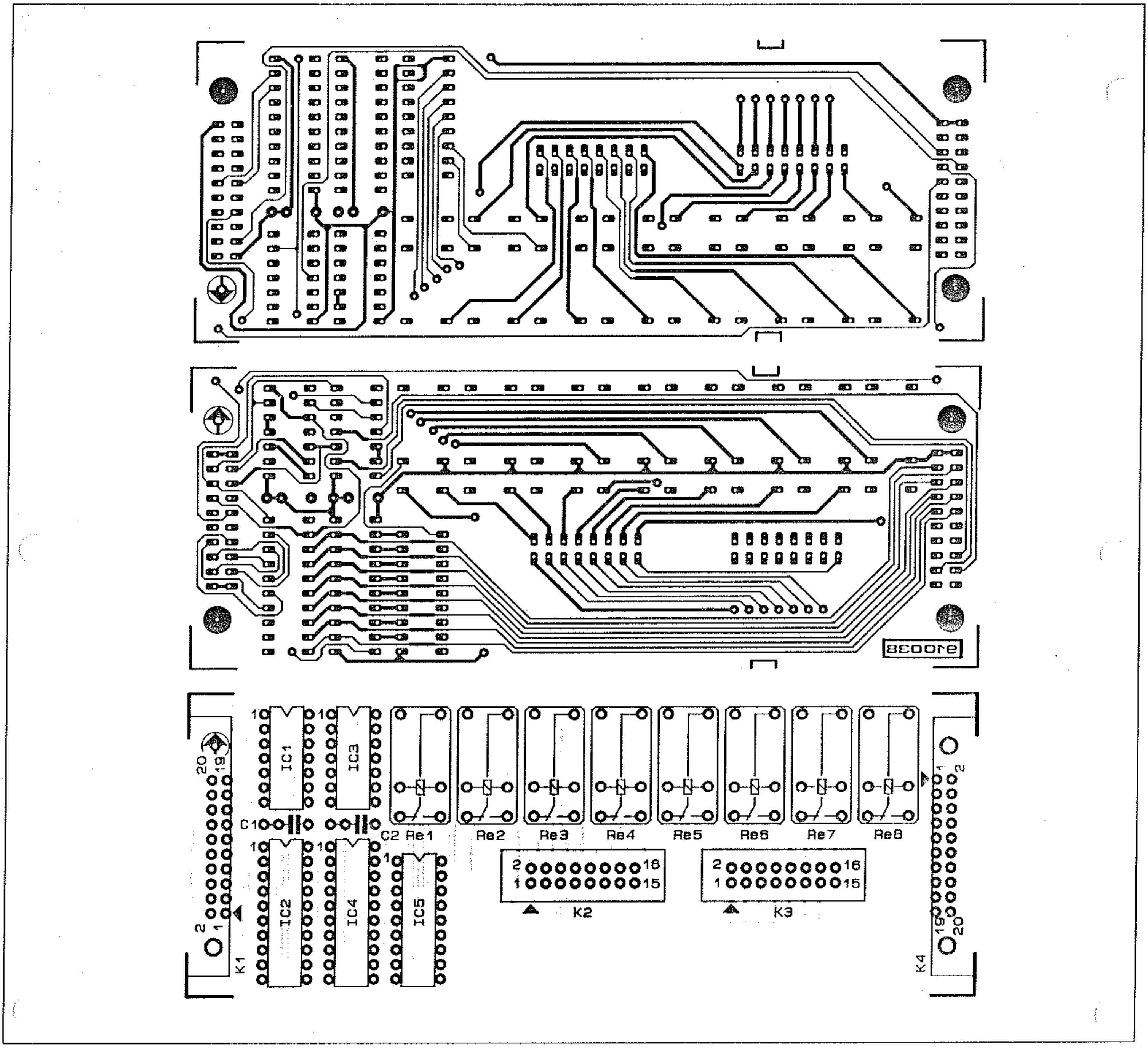


Fig. 2. Printed-circuit board for the relay card. Note that this board is double-sided and through-plated.

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10 CLS
20 ' ........................................................ ibmio interface test
30 X=0 ' .................................................... address definition
40 ' .......... X=0: &H300-&H303 X=1: &H304-307 X=2: &H308-&H30B X=3: &H30C-30F
50 ' .......... X=4: &H310-&H313 X=5: &H314-317 X=6: &H318-&H31B X=7: &H31C-31F
60 X=&H300+X*&H4
70 ' .................................................................. addresses
80 A1=X+0: A2=X+1: A3=X+3: A4=X+2: ' ............................. I/O addresses
90 ' ................................A1 - A4 = relay card 1  to  relay card 4
100 ' ................................................... test of I/O ports
110 CLS
120 PRINT "Testing I/O"
130 FOR I=0 TO 7
140 OUT A1,2^I ' ............................. close relay number i of card 1
150 OUT A2,2^I ' ............................. close relay number i of card 2
160 OUT A3,2^I ' ............................. close relay number i of card 3
170 OUT A4,2^I ' ............................. close relay number i of card 4
180 GOSUB 280  ' ................................................... wait
190 NEXT I
200 FOR I=0 TO 7
210 OUT A1,255-2^I ' ......................... open relay number i of card 1
220 OUT A2,255-2^I ' ......................... open relay number i of card 1
230 OUT A3,255-2^I ' ......................... open relay number i of card 1
240 OUT A4,255-2^I ' ......................... open relay number i of card 1
250 GOSUB 280      ' ............................................... wait
260 NEXT I
270 GOTO 130 ' ..................................... return for next cycle
280 ' ................................... subroutine to execute a wait period
290 FOR J=0 TO 1000:NEXT
300 RETURN
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Fig. 3. Run this little BASIC program to test one to four relay cards.

COMPONENTS LIST

Capacitors:

2	100nF	C1;C2

Semiconductors:

1	74HCT32	IC1
1	74HCT245	IC2
1	74HCT04	IC3
1	74HCT574	IC4
1	ULN2803	IC5

Miscellaneous:

2	20-way pin header with side latches	K1;K4
2	16-way pin header	K2;K3
8	PCB mount relay V23040-A0001-B201 (Siemens)	Re1-Re8
1	enclosure (e.g., Heddic 222)	
1	Printed circuit board	910038

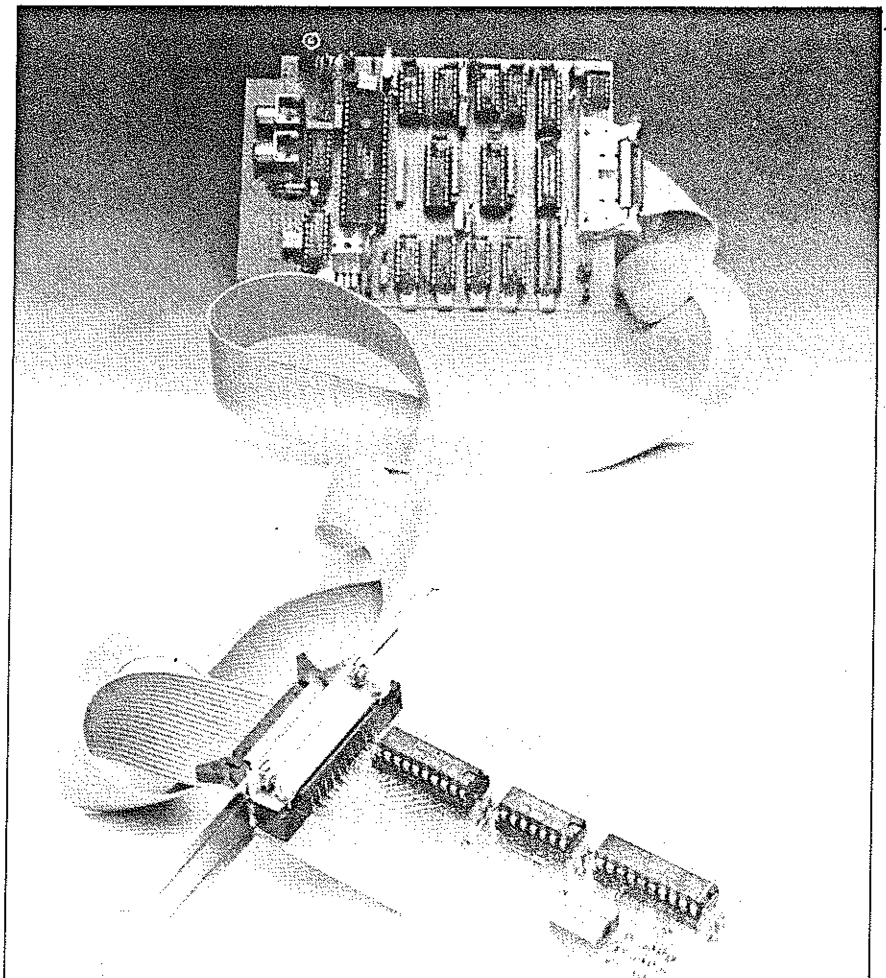
UNIVERSAL I/O INTERFACE FOR IBM PCs

Those were the days when you could use your Commodore C64, Acorn Atom or ZX81 computer to control hardware intelligently. Model train systems, robots, greenhouse watering and temperature control systems — all within easy reach of the keen programmer with little or no knowledge of computer hardware. Alas, the coming of the IBM PC, the compatibles, the ATs and the 386-based systems, seems to have banished simple hardware interfacing, the PC being an expensive 'box' harnessing a lot of computing power, but restricted to use in an office environment. We do not agree that a PC is unsuitable for control applications: all it needs is the circuit described here: a low-cost fully buffered insertion card that forms a versatile, simple and safe link between the PC (whether an XT, AT or 386-based machine) and your own hardware.

A. Rigby

USING a computer and some home-brew software to control apparatus is sheer fun. A few lines of program code allow lamps to light, motors to start turning, and model trains to find their way on a complex track system. Sensors and other types of recorder device enable a computer to measure and store physical quantities from the 'real world' around us.

Unfortunately, an IBM PC or compatible appears to be less suitable for the above control applications as it is very much a closed system designed for office use. Does that imply that we have to say goodbye to the model train system and the computer-controlled hobby lathe? No! Many of you will have noted that PC interface cards are being offered for industrial control applications. Unfortunately, these cards are pretty expensive, so it's time for a low-cost solution.



Count the components

The circuit shown in Fig. 1 may well be the simplest PC I/O interface you have ever seen, having only three ICs, three resistors and three capacitors. The interface is suitable for all types of IBM PC and compatibles, i.e, XTs, ATs and 386-based systems.

The circuit acts as a buffer between the computer and the external hardware, and is set to operate at a unique address in a small area in the PC's I/O range.

As shown in the circuit diagram, the connector between the computer and the interface card is a type with 31 connections at each side. This is the well-known IBM PC expansion slot connector. A small number of signals available on this connector are used for the present interface and/or the hardware controlled by it. The external hardware is connected to K1, a 20-way PCB header that provides the 8-bit wide databus, two address lines, an enable signal and the read and write signals. The computer's 5-V supply rail is also available on K1, allowing small (experimental) digital circuits to be powered without the need of an external supply.

The address decoding logic ensures that interface card occupies four addresses in the I/O range reserved for prototyping cards. The actual address setting is accomplished with three switches in DIP switch block S1. In all cases, a free base address must be used, i.e., the interface card must not share an I/O address with any other card in the PC. The four addresses in the block are selected individually by A0 and A1. For convenience the DIP switch settings are printed on the component overlay of the interface card (see the component mounting plan in Fig. 2b).

The three switches determine the logic level at inputs P0, P1, P2 and P3 of IC1. The pull-up resistors connected to these inputs provide a logic high level when a switch is opened. When a switch is closed, the relevant IC input is logic low. All other P inputs of IC1 are held at fixed logic levels.

Address lines A2 to A9 on the expansion bus are connected to inputs Q0 to Q6 of address comparator IC1. An AND gate, IC3d, combines address lines A8 and A9 at input Q6. This frees input Q7 for use by AEN, the address enable signal that indicates DMA (direct memory access) activity without an I/O address being decoded. Gate IC3c ensures that IC1 is enabled during a read or write operation only. When the binary code at the P inputs equals that at the Q inputs, output $\overline{P=Q}$ goes low. This signals the selection of the user hardware hooked up to connector K1. The $\overline{P=Q}$ output also actuates the $\overline{G}$ input of IC2, which enables the PC's databus to be connected to the databus on K1. The direction of the dataflow between the PC and the external hardware is determined by the level of the $\overline{RD}$ (read) signal. A low level means that data is transferred from K1 to the PC, while a high level means data transfer from the PC to K1. Both the $\overline{RD}$ and the $\overline{WR}$ (write) signal on connector K1 are provided by the PC and buffered by a gate, IC3a and IC3b respectively. The PC's databus is buffered by IC2. Since all PC signals are buffered, the risk of cross-effects between the PC and the external hardware is reduced to a minimum.

Construction

The compact printed-circuit board designed for the PC interface is shown in Fig. 2. Ready-made boards supplied through our Readers Services are provided with gold-plated bus contact fingers. Connector K1 is a so-called box header with right-angled PCB pins. It protrudes from a clearance cut in the support bracket attached to the rear side of the circuit board. This arrangement allows ready connection of a flatcable with an IDC connector.

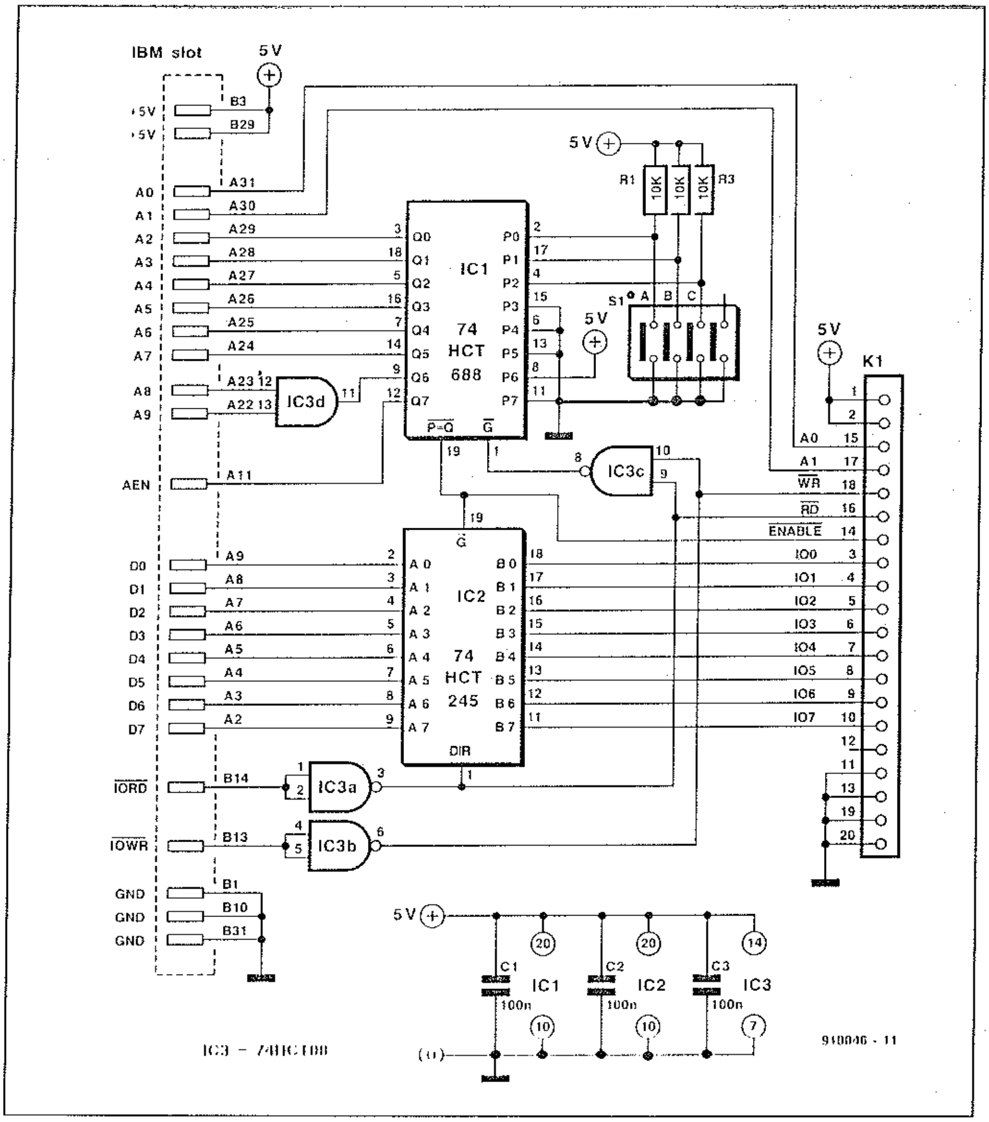


Fig. 1. Circuit diagram of the interface card for IBM PCs and compatibles. This ultra-simple circuit forms the ideal link between a PC and your own hardware developments.

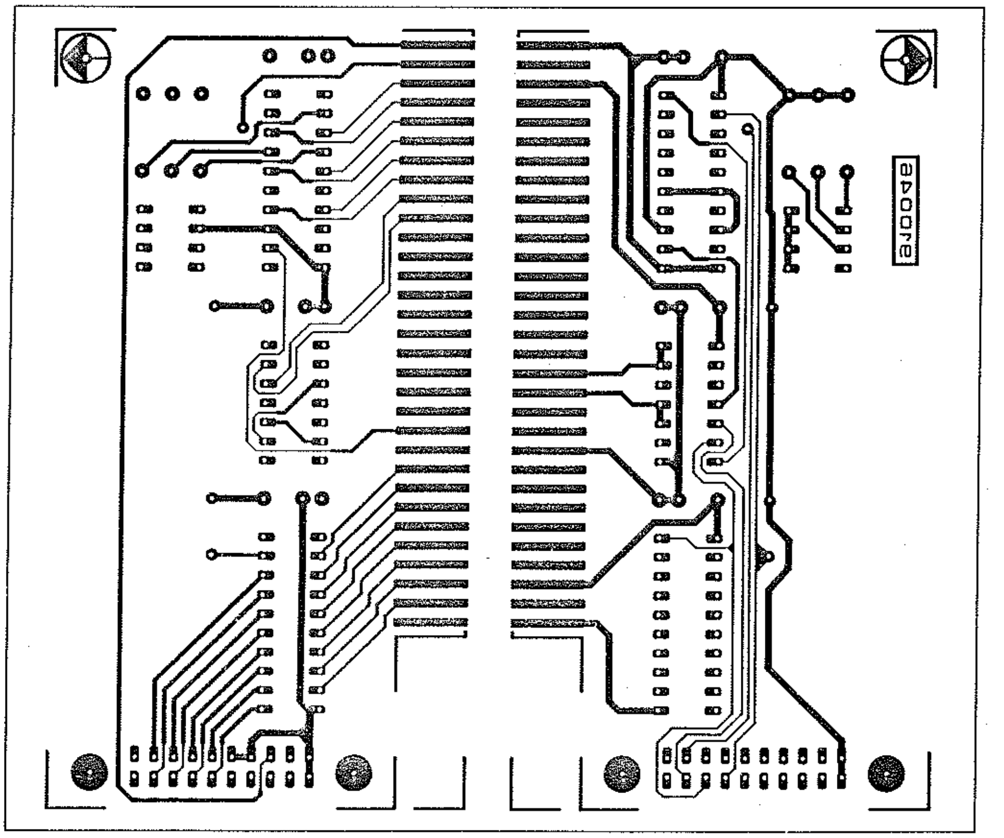
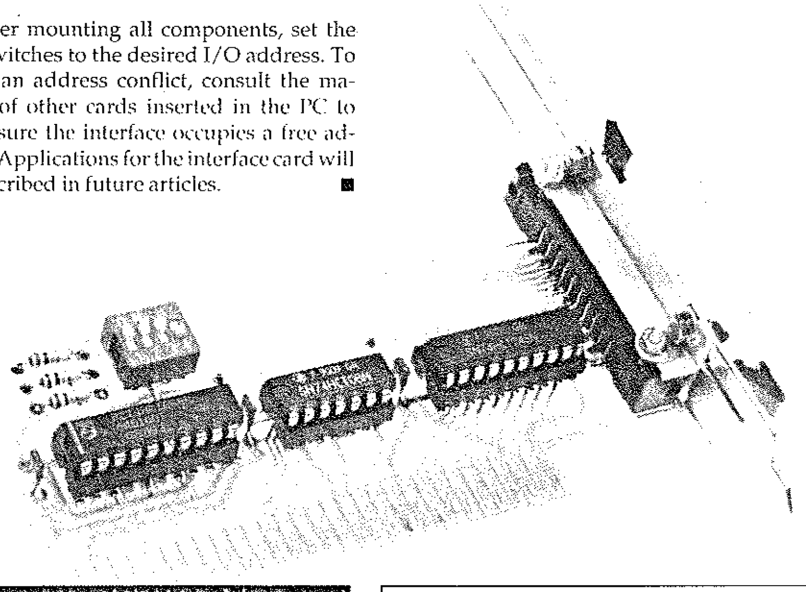


Fig. 2a. Mirror-image track layouts of the PCB component side and solder side.

After mounting all components, set the DIP switches to the desired I/O address. To avoid an address conflict, consult the manuals of other cards inserted in the PC to make sure the interface occupies a free address. Applications for the interface card will be described in future articles. ■



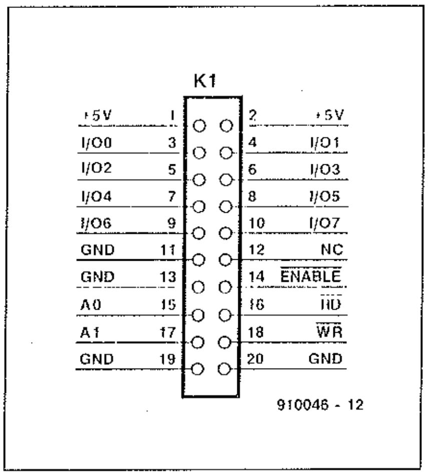


Fig. 3. Pinning and signal assignment on connector K1.

COMPONENTS LIST

Resistors:
3 10kΩ R1;R2;R3

Capacitors:
3 100nF C1;C2;C3

Semiconductors:
1 74HCT688 IC1
1 74HCT245 IC2
1 74HCT08 IC3

Miscellaneous:
1 20-way header with eject handles and angled PCB pins K1
1 4-way DIP switch S1
1 printed-circuit board 910046

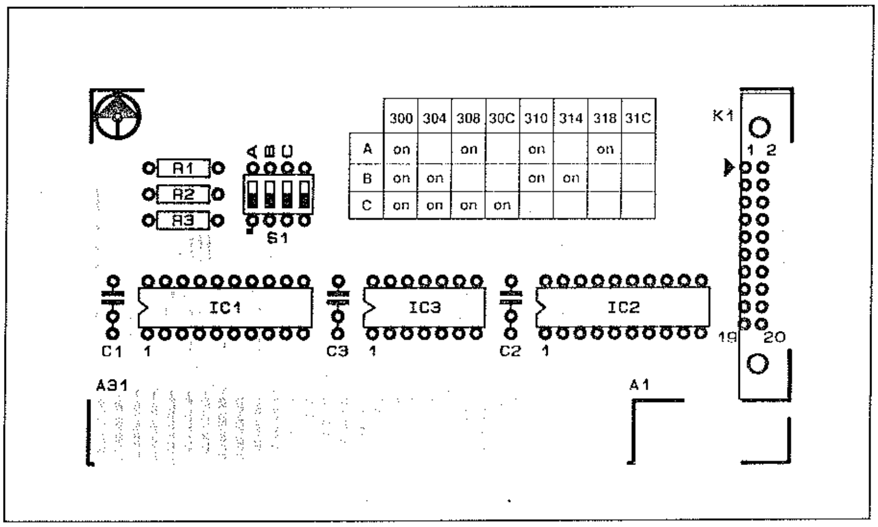


Fig. 2b. Component mounting plan.

NEW PRODUCTS

Floppy disk emulator for PCs

The recently introduced EDISK insertion card from DSS innovative electronics is capable of emulating a floppy disk drive in a PC. The maximum storage capacity of the EDISK is 4 MBytes with EPROMs fitted, or 1 MBytes with static RAMs fitted. The following EPROM types may be used: 27(C)512 (64 KBytes); 27(C)010 (128 kBytes); 27(C)020 (256 kBytes); 27(C)040 (512 kBytes). The card supports two 32 kByte SRAM types, the 62256 and the 621000.

The EDISK card enables you to replace the mechanical floppy disk drive A: by an all solid-state equivalent, which will be faster as well as more reliable, offering a speed of the order of a RAM disk. The main difference between the EDISK and a RAM disk, however, is that the contents can be stored in non-volatile EPROMs, or stored in static RAM. When the computer is switched off, the programs contained in the EDISK will be retained in static RAM by virtue of a back-up battery. Another difference is that the EDISK is automatically write-protected if EPROMs are used. The EPROMs are loaded with the aid of a programmer; their content can not be changed or erased by the PC user.

Since the EDISK is based on non-volatile memory, it is possible to boot the computer without a floppy disk, or even without a disk controller card.

The EDISK allows a combination of EPROMs and RAMs to be fitted, which effectively emulates two drives, drive A: containing EPROMs and drive B: SRAMs.

Applications of the EDISK include a 'stripped' XT computer that can be connected to a network as a diskless station. Alternatively, a motherboard fitted with an EDISK and a special I/O card can form a powerful control system. The use of SRAMs allow system parameters to be stored and altered as required.

For more information on the EDISK contact

DSS innovative electronics • Accustraat 25 • 3903 LX Veenendaal • Holland. Tel. +31 8385 41301. Fax: +31 8385 26751.