Interfacing via the pc's printer port, this 16-channel data-capture subsystem with 12-bit resolution can be moved between machines without having to open the computer's lid. In addition to its analogue inputs, the subsystem also provides an eight-bit digital output port, as Pei An explains.

CATCHING DATA VIA LPT1

The present precision data acquisition system has a 16-channel analogue multiplexing facility and a 12bit a-to-d conversion accuracy. It incorporates an on-board digitally-controlled variable gain amplifier, offering gains of 10, 100 and 1000.

Input voltage is in the range from –5V to +5V with an accuracy of about 1μV. The conversion rate is 7Hz. In addition, the system has an 8-bit digital output port. This allows the device not only to read analogue signals into the computer, but also to send data out of the computer for controlling external equipment.

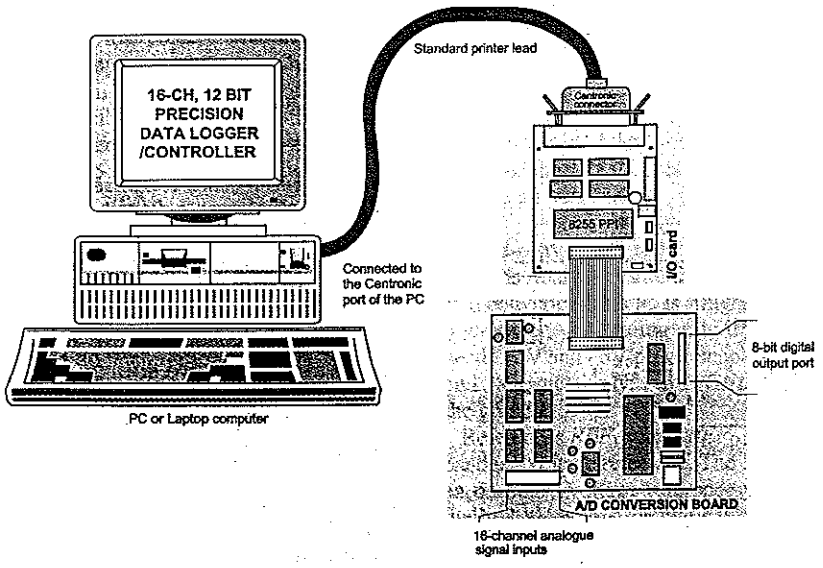
There are two main modules in the data logging system – an a-to-d conversion board and an interfacing card. The former deals with analogue signal multiplexing, amplifying and analogue-to-digital conversion; the interfacing card manages communication between the a-to-d board and the computer.

I have designed two versions of the interfacing cards. The first is intended for interfacing with the centronics port of the computer and the second for interfacing with the RS232 ports. Both cards incorporate an *8255* programmable peripheral interfacing (ppi) IC. This provides three programmable eight-bit i/o ports through which the a-to-d converter board is connected. In this article, only the design of the centronics i/o card is discussed.

The a-to-d board can be connected to any i/o ports, provided that two 8-bit outputs and one 8-bit input are available. A complete data logging system connected to a pc or a laptop computer is illustrated in **Fig. 1**.

The description of this system is divided into two parts. The first one concentrates on the works of the a-to-d conversion board and the second on the centronics i/o card.

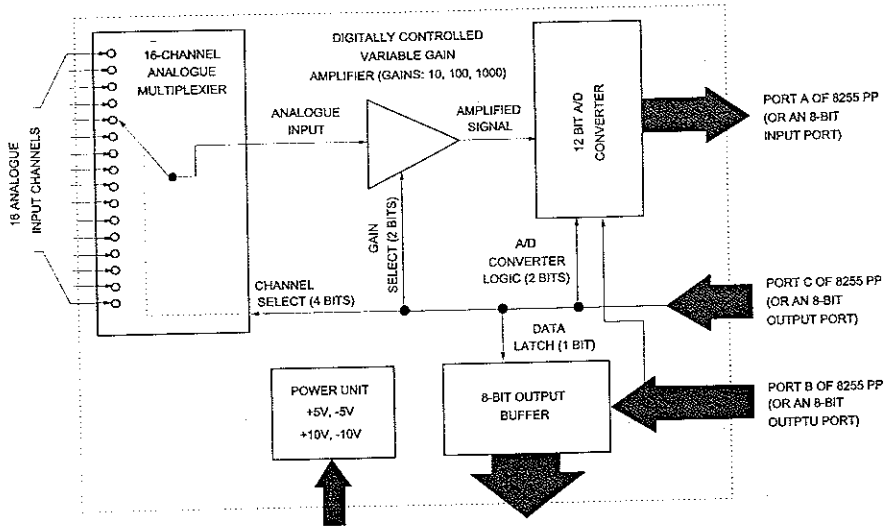
Fig. 1. Precision data logger/controller comprises an a-to-d converter board providing 16 analogue input lines and 8 ttl outputs. It is controlled by a pc or laptop computer via the centronics printer port using appropriate i/o card.



A-to-d conversion module

The system comprises five blocks. These are the analogue multiplexer unit, the digitally-controlled variable gain amplifier unit, the a-to-d conversion unit, the digital output unit and power supply unit. **Figure 2** shows the block diagram of the a-to-d board while **Fig. 3** gives the circuit diagram.

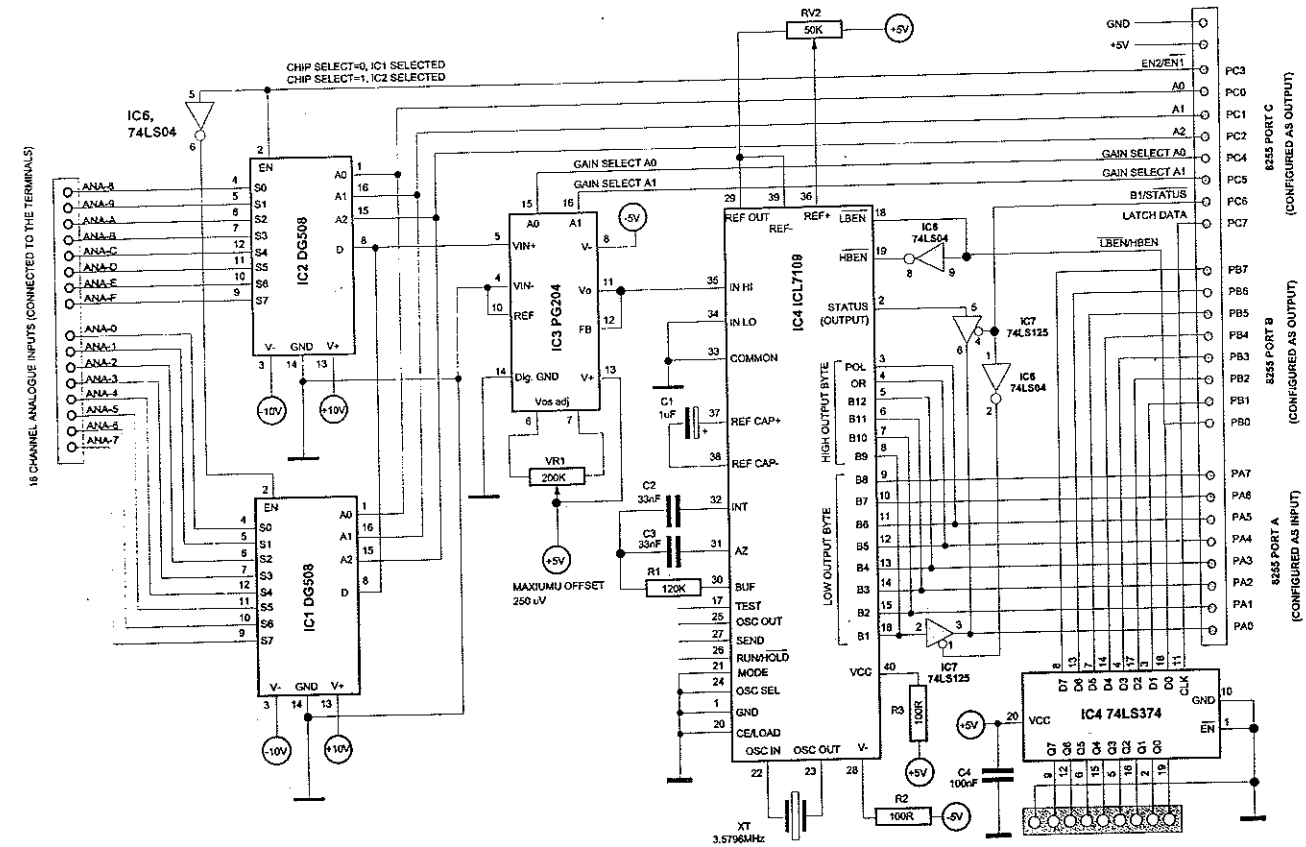
Analogue multiplexer. The analogue multi-



plexer unit is built around two *DG508* eight-channel analogue multiplexer ICs, namely $IC_{1,2}$. These provide 16 channels of analogue inputs.

The *508* is a high quality analogue switch exhibiting very low on resistance and high off resistance. On resistance is virtually constant over the entire analogue signal range. The IC can handle analogue input voltages up to ±40V. A dual balanced power supply is needed. Supplies V+ and V– connect to the +10V

Fig. 2. Block diagram of the a-to-d conversion board. One of the 16 analogue inputs is selected by the analogue multiplexer. The selected signal is first amplified by the digitally-controlled variable gain amplifier, then fed into the 12-bit a-to-d converter. Data from the computer is stored in the output buffers. The board communicates with the pc via one 8-bit input port and two 8-bit output ports.



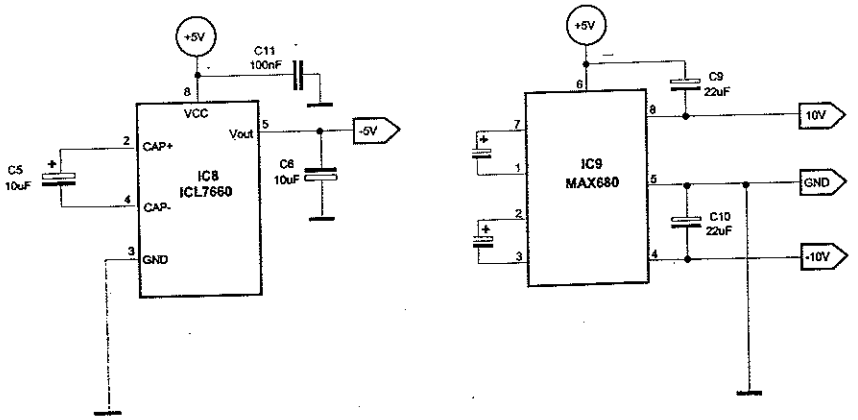


Fig. 3. The a-to-d board comprises two analogue multiplexers, a digitally-controlled variable gain instrument amplifier, a 12-bit a-to-d converter and support ttl chips. Output data from the pc is latched in the 374 octal D-type latches.

Software/hardware source

Printed circuit boards, control software and parts for the a-to-d converter and centronics or RS232 interfacing cards are available from the author. For more details, write to Dr An at 58 Lamport Court, Lamport Close, Manchester M1 7EG, England, or phone or fax on +44 (0)161 222 8279.

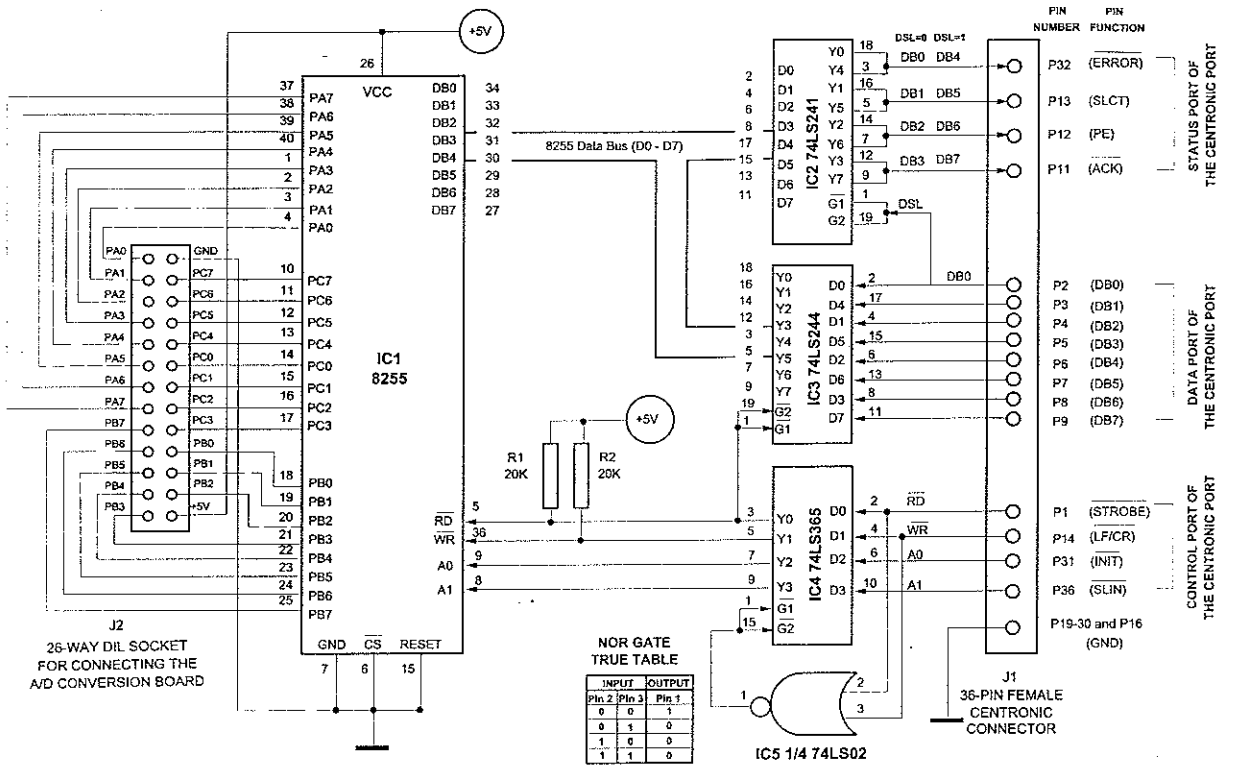


Fig. 4. Centronics port to 8255 peripheral interface chip. Communication between the computer and the 8255 is achieved by several ttl chips. Data and status ports centronics interface are used for sending data to and reading data from the 8255 peripheral IC. The control port manages operation of the 8255 peripheral chip.

and –10V rails of the power supply. Pins S_0 through S_7 are the analogue inputs while D, on pin 8, is the analogue output.

Analogue input is selected by applying an address at $A_{0\text{-}2}$ address lines. During the operation, the enable input should be pulled high. Address lines $A_{0\text{-}2}$ are connected to the lines $DB_{0\text{-}2}$ on port C of the *8255* peripheral IC. Enabling for IC_2 connects directly to DB_3 of port C and the enable for IC_1 connects to DB_3 via inverter IC_6. This ensures that only one multiplexer works at a time.

Analogue outputs of the ICs are wired together and then connected to the input of the amplifier, Fig. 3.

Variable-gain amplifier. Analogue outputs from the multiplexers connect to the input of the *PGA204* amplifier. This device is a high performance, low cost, general purpose instrumentation amplifier with programmable gain. It is laser trimmed for very low offset voltage and drift combined with high common-mode rejection. In addition, it will operate with supplies from 4.5 V to 18 V and its quiescent current is about 5mA.

Inputs V+ and V– of the *PGA204* connect to the +5V and –5V rails of the power supply. Gains of 1, 10 100 and 1000 are digitally selected by two ttl/cmos-compatible address lines, $A_{0,1}$ on pins 15 and 16.

There is no latching for the address lines. A change in the address inputs immediately selects the new gain. However, a delay of around a microsecond is needed for the amplifier to settle to a new output voltage in the newly selected gain.

Input connects between V_{in-} and V_{in+}. Internal input protection allows overloads up to ±40V on the inputs without damage. Output V_o is referred to the output reference *REF*, which normally connects to the analogue ground via a low impedance.

The *PGA204* has an output feedback connection at pin 12 which must be connected to the V_o output terminal for proper operation. Normally, a constant current of approximately 1.3mA flows through the digital ground pin. This makes it necessary to return the digital ground through a separate connection path so that the analogue ground is not affected by current in the digital ground.

Pins 6 and 7 allow offset of the input stage to be trimmed. Address lines $A_{0,1}$ connect to $BD_{4,5}$ of the *8255*'s port C, which is configured as an output port.

A-to-d conversion unit. Amplified analogue signal is finally fed into the *ICL7109* 12-bit a-to-d converter. This IC is a high-performance, low-power, integrating a-to-d converter. It needs +5V and –5V power supplies on pins 40 and 28 respectively. Pin 1, *GND*, connects to the ground.

References REF_{IN+} and REF_{IN-} connect to a bandgap voltage reference. The *7109* provides an on-board voltage reference which is normally 2.8V below V+ and has a typical temperature coefficient of ±80 ppm/°C. This reference voltage is at REF_{OUT}.

The IC needs some capacitors and resistors for the analogue side of the converter, values of which should be calculated according to the manufacturer's data sheet. An on-chip oscillator operates with an inexpensive 3.5795MHz tv crystal producing 7.5 conversions per second.

Digital communication with the *7109* is configured in direct mode, achieved by making the mode input pin open or low. In this mode, output data is directly accessible under control of the chip. The *RUN/HOLD* pin is unconnected and thus pulled high by the *7109*'s internal pull-up resistor. This allows the converter to perform a-to-d conversions continuously and to update the 14 tri-state outputs $B_{1\text{-}12}$, *OR* and *POL*. Lines $B_{1\text{-}12}$ present the 12 bits of the conversion data. Input over-ranging is indicated on the *OR* pin while *POL* indicates polarity of the signal.

During a conversion cycle, the status output goes high then low after new converted data has been stored in the output latches. It is used as a 'data-valid' flag for monitoring the status of the converter. In this design, *STATUS* and data bit B_1 share the same line, which connects to DB_0 of port A of the *8255* peripheral interface. Data line DB_6 of port B selects whether *STATUS* or B_1 is read into the pc.

Chip enable line *–CE/LOAD* connects to the ground to enable the IC. When *–LBEN* is low, the low eight bits $B_{1\text{-}8}$ output the data while high bits $B_{9\text{-}12}$, *OR* and *POL* are high impedance. When *–HBEN* is low, $B_{9\text{-}12}$, *OR* and *POL* will output data and the low bits are in high-impedance state.

In Fig. **3a**, some outputs in the two groups are connected together to form an eight-bit

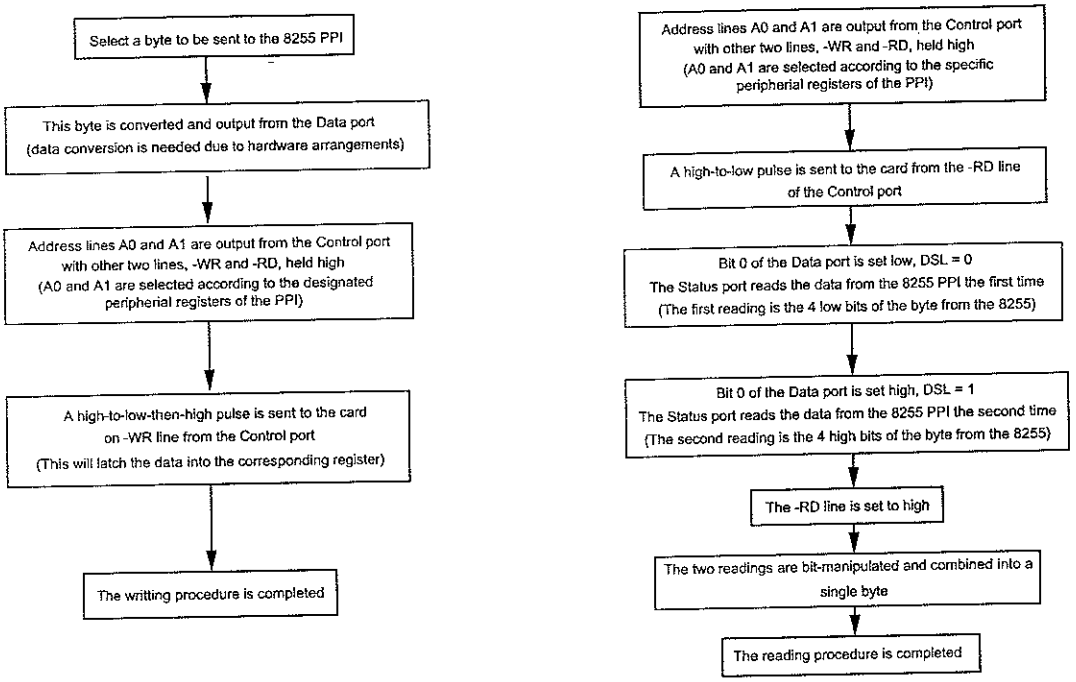


Fig. 5. Software flow for writing data to, and reading data from, the peripheral registers of the 8255 parallel interface. When writing, the data port of the centronics interface supplies data to the 8255 and the control port controls transfer. During reading, data from the 8255 is read into the pc via the status port. As only four inputs are used by the status port, the eight-bit data is loaded into the pc in two consecutive readings, which is controlled by the first lsb of the data port. Operation of the 8255 is again managed by the centronics control port.

output instead of 14 bits. Lines *–HBEN* and *–LBEN* are used to select the lines either in the high byte or in the low byte. These eight-bit data buses connect to port A of the *8255* peripheral interface which is configured as an input port. Line *–HBEN* connects to DB_0 of port B while *–LBEN* connects to DB_0 of port B via inverter IC_6.

Digital output unit. An *LS374* octal latch is used. Inputs to the IC are supplied by port B of the *8255*, which is configured as an output. This data is latched to the outputs by taking the clock line from low to high. The clock is connected to BD_7 of the *8255*'s port C.

Power unit. The power unit derives –5V and ±10V dc supplies from a 5V dc rail via two voltage conversion chips, Fig. **3b**. The *ICL7660* converts +5V to –5V while a *MAX680* converts +5V to +10V and –10V.

Interfacing to the pc

Interfacing via the centronics printer port was discussed in an article entitled '*Real world control via LPT*' in the September issue of *EW+WW*. Briefly, the centronics port consists of three independent ports, namely, the data

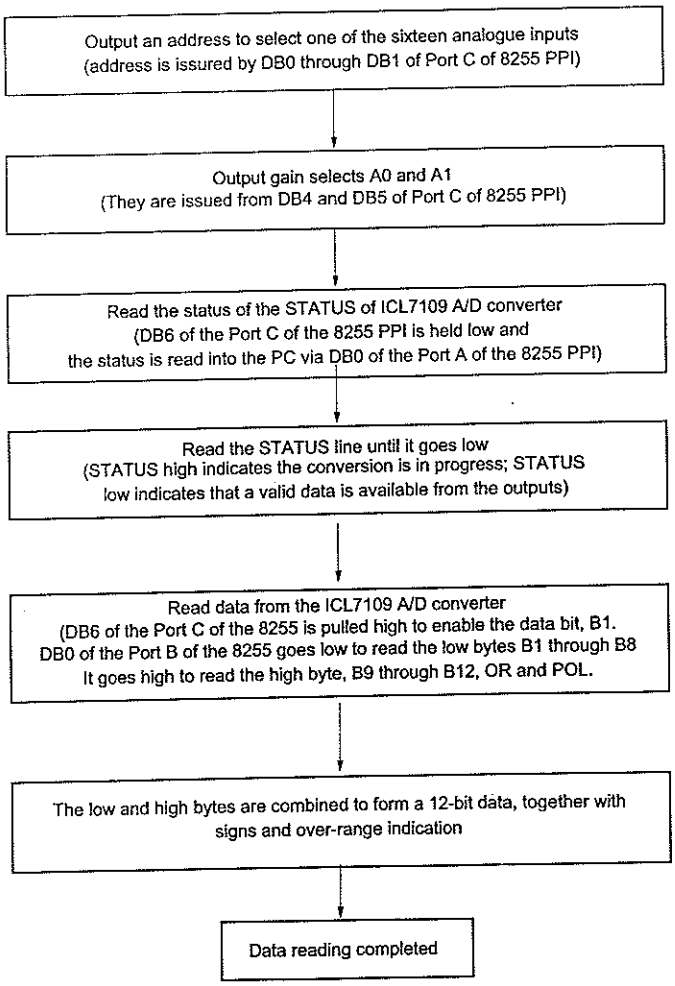


Fig. 6. Analogue-to-digital conversion begins with selecting one of the 16 analogue inputs. It is followed by sending a command to select the gain of the amplifier. After this the status of the a-to-d converter is polled continuously until it indicates that conversion is finished. The 12 bit data – plus polarity and over-range flags – are read into the pc twice. They are finally combined to form a single 12-bit word.

output port, the control output port and the status input port.

For the data logger, the centronics data port is used to send information to the interface card while the status port is used to read data from the IC. The control port manages reading and writing operations of the *8255* interface chip.

The *8255* is an industry standard programmable peripheral interface with four internal registers. Three of these are called peripheral registers and are associated with ports A, B and C. The fourth is the control register.

All three peripheral registers are used for data transactions between the *8255* and external circuits while the control register is used to initialise the operation modes of the parallel interface.

There are eight bidirectional data lines, $DB_{0\text{-}7}$, through which data is written to or read from the internal registers under the control of read and write lines. Address lines $A_{0,1}$ select a particular register.

Data transfer is facilitated by IC_2 and IC_3, which are tri-state buffers. Control over the *8255* is made by IC_4 and IC_5 which are a tri-stage buffer and nor gate respectively.

You can see from **Fig. 4** that two lines of the centronics control port, pins 31 and 36, are connected to address lines $A_{0,1}$ of the *8255* peripheral interface via IC_4 – a tri-state buffer.

The other two lines of the control port, pins 1 and 14, connect to *–RD* and *–WR* of IC_1 via IC_4. A problem could occur when these two lines are both low, since the *8255 –RD* and *–WR* lines cannot be set low simultaneously. To prevent this, a nor gate is used. Its two inputs connect directly to the two control lines from the centronics port, pins 1 and 14, and its output connects to the enables of IC_4.

When the two lines from the control port are both low, output of the nor gate goes high. This disables the buffers on the *LS365* and sets all the outputs at high impedance. Resistors $R_{1,2}$ pull the *–RD* and *–WR* lines high.

To write data to an *8255* register, firstly the required data is written to the centronics data port together with an address to the control port, then a high-to-low-then-high pulse is issued from the control port write line. This enables data on the inputs of IC_3 buffers to be transferred to the *8255* data bus and in the same time written into the selected register.

Reading data from the *8255* is slightly complicated, since the centronics port only has five input lines. In order to read eight bits of data, the computer has to read at least twice. This is done by IC_2, an *LS241* tri-state octal buffer.

In Fig. 4, when the first enable, pin 1, is low, the four left hand side buffers work, i.e. the outputs follow the inputs. When pin 19, the second enable, goes high, the four right-hand side buffers operate.

By connecting pins 1 and 19 together to form a data-select line and by putting the line low and then high, the status port can read the four bits connected to the left and right hand buffers in turn. These two readings are then bit-manipulated and combined to form a single eight-bit byte.

Operating in such a manner, the 8-bit data appearing on the input lines of IC_1 can be read into the centronics port. Referring to Fig. 2, the data-select line is controlled by DB_0 of the centronics data port.

The card incorporates a *7085* 1A, 5V regulator. An external 8-12V dc supply capable of delivering about 100mA is needed. In my design, the regulated 5V supply also feeds the expansion socket for conveying power to the a-to-d conversion board. An 800mA on-board fuse is used.

Programming

I have written a control program in *Turbo Pascal 6* for this data logging system. Flow charts for the centronics i/o card and data logging system are shown in **Figs 5** and **6**. ■