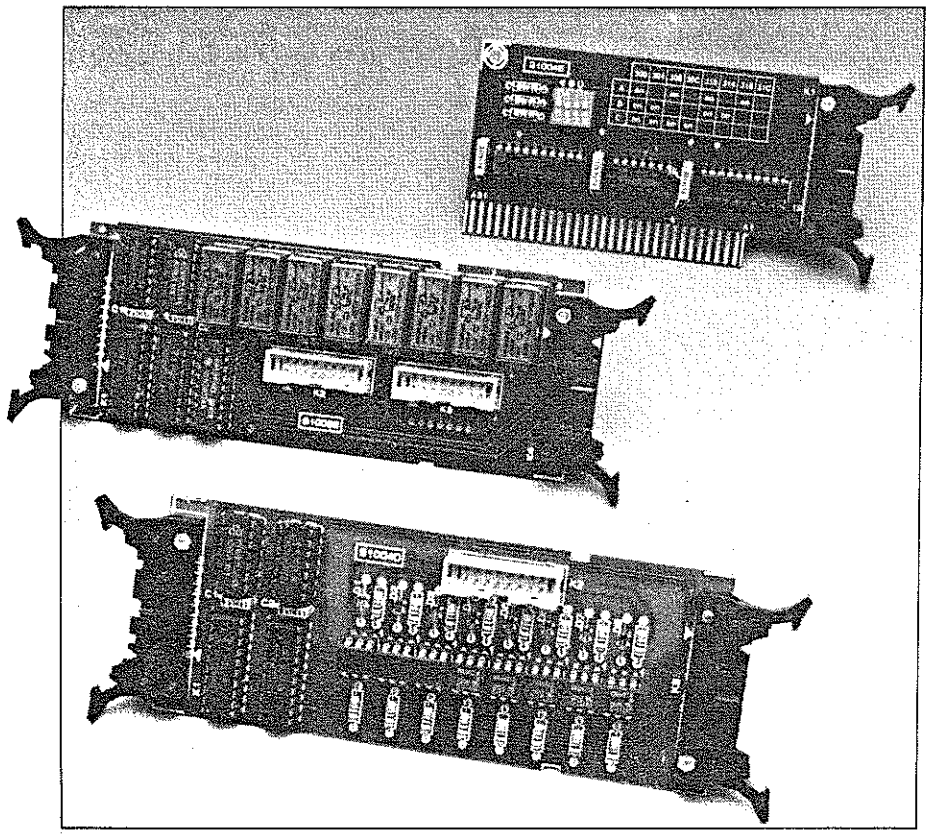
OPTO CARD FOR UNIVERSAL PC I/O INTERFACE

Whenever an interface is connected to a circuit with a supply voltage higher than 5 V, there is the risk that an error during experimenting, or a faulty component, will cause serious damage to the computer system. The opto card described here has been designed to afford complete electrical isolation between the computer and the (cruel) outside world, which is the only way to prevent system down time and expensive repairs caused by incompatible signal levels.

Design by J. Ruiters

IN this article we present the second extension card for the Universal I/O Interface For IBM PCs, described in Ref. 1. While the relay card for this bus (Ref. 2) offers electrically isolated outputs, the present opto card is designed to process input signals in the safest possible way. By the way, the multi-purpose Z80 card described elsewhere in this issue may also be used as a controller for the universal bus.



Eight optocouplers

The circuit diagram of the opto card is given in Fig. 1. If you compare it with the circuit diagram of the relay card, you will find quite a few similarities. That is not surprising, because the functions of the two cards are closely related, one being a parallel output device (relay card), the other a parallel input device (opto card). The address decoding logic, for instance, is identical, consisting of a number of gates and a bidirectional buffer. With reference to Fig. 1, we are talking of IC9, IC10 and IC12. How the card is addressed, that is, how it complies with the rules of extension card addressing that apply in the universal bus system, will be reverted to below.

The opto card is actuated when bus signals A0, A1, $\overline{RD}$ and $\overline{ENABLE}$ go logic low. Consequently, bus buffer IC10 is enabled, and data is conveyed towards connector K1, i.e., towards the PC. At the same time, the $\overline{OC}$ input of data latch IC11 is pulled low, which enables the latch outputs. The data on the databus is clocked into the latches on the negative (falling) edge of the $\overline{OC}$ signal. This means that data applied to the optocoupler inputs is captured right at the start of a read cycle of the computer system, which ensures that data is stable on the bus during the actual read operation.

The eightfold optocoupler input circuit is all plain sailing. The only parameters to keep in mind are a couple of maximum specifications. To begin with, the input voltage is limited to 'low voltage' (in most countries, this is defined as 42 V a.c., or 60 V d.c.). This limitation is not caused by the optocouplers, but rather by the printed circuit board and a few other components. When designed to handle the 240 V (110 V) mains voltage at the input, the PCB would have become much larger to meet the relevant safety requirements. A further point to note is the specification of the series resistors with the optocouplers (R2, R4, R6, R8, R10, R12, R14 and R16). The indicated resistors (1 kΩ, 0.25 W) may be used when the input voltage is between 2 V and 15 V d.c. Each optocoupler is protected against reverse voltages by a diode connected in anti-parallel. If voltages greater than 15 V d.c. are applied to the inputs, the

series resistors have to be increased accordingly, or resistors with a higher permissible dissipation must be used. The latter solution is not very elegant because of the larger size and the heat developed. The resistor values are calculated such that the LED current is a few milli-ampères at the given input voltage.

The construction of the opto card is entirely straightforward, and therefore not discussed further.

The bus system

As shown in Fig. 2, the address of any extension card connected to the universal bus system is determined by its position in the chain of extension cards. Unconventionally, DIP switches, jumpers and the like are not used. Apart from the beautifully simple and inexpensive hardware, the advantage of this system is mainly that you can not make address setting errors because there is nothing to set: the card address is determined by its physical position in the system. Note, however, that you must not confuse the bus-IN and bus-OUT connectors. Remember, the incoming A0 signal is inverted on every extension card, and swapped with A1 on the bus-OUT connector. This is done to enable any extension card to be selected when both A0 and A1 are logic low, although the actual address to be supplied by the PC to select a particular card is determined by the number of cards connected ahead of that card.

Those of you who have recalled from the earlier articles that the bus system has only four addresses may be surprised to see eight extension cards in Fig. 2. This is simple to explain. Any bus address can be read from, or written to. In other words, there are four 'read' addresses, and four 'write' addresses, which makes a total of eight. This difference is of no consequence as long as you do not wish to use more than four cards, which can then be chained via linking cables without problems. The difference between reading and writing is not in order until you use more than four cards. Let us assume that you wish to hook up four relay cards and four opto cards. This requires the positions with the same card number, e.g., 1 and 1', to be occupied by one relay card (write only) and one opto card (read only). You can not fit two

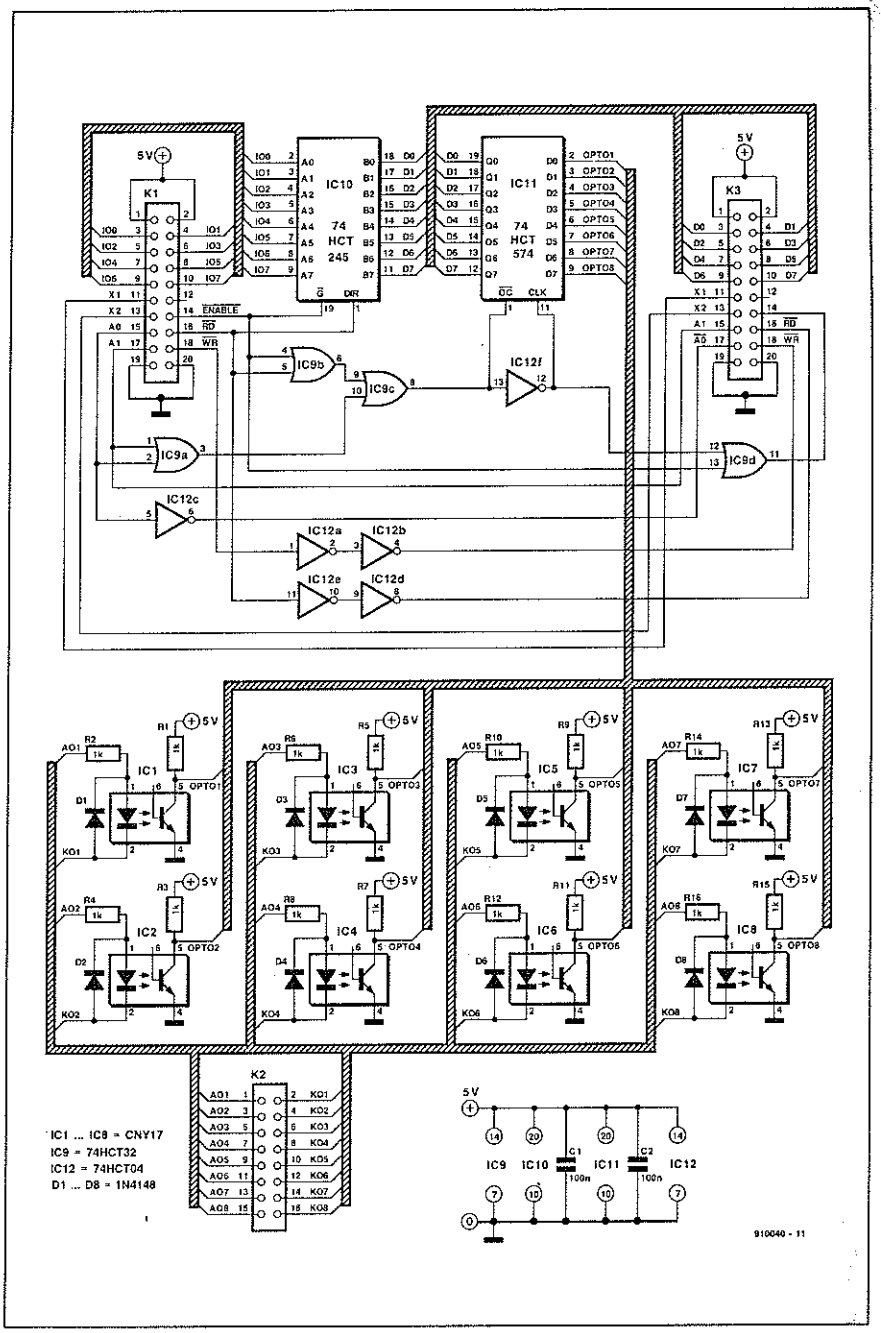


Fig. 1. Eight optocoupler inputs ensure that input signals can not cause damage to the computer.

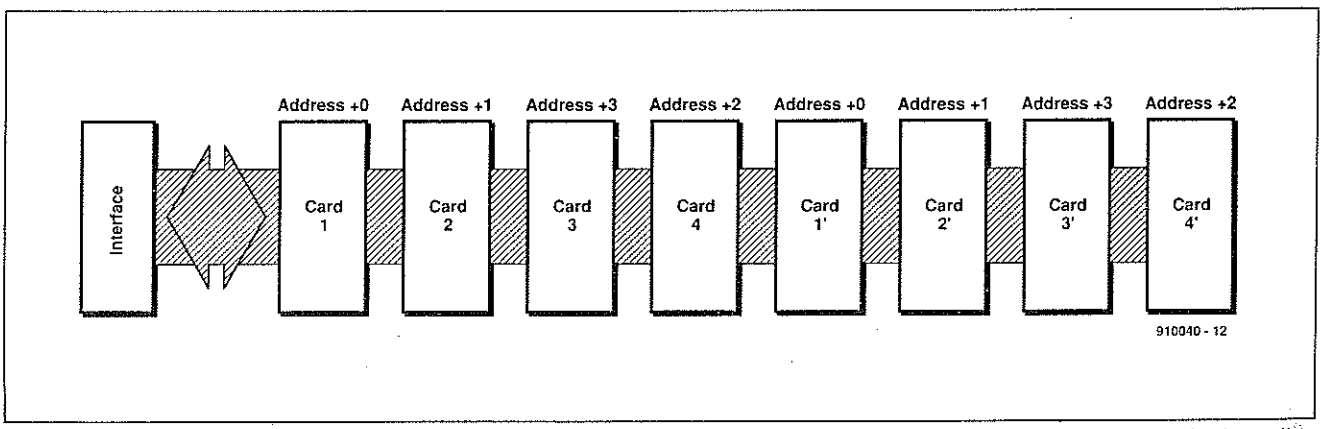


Fig. 2. The bus system can always accommodate four extension cards. However, it is also possible to fit up to four more cards, depending on their type (read or write function).

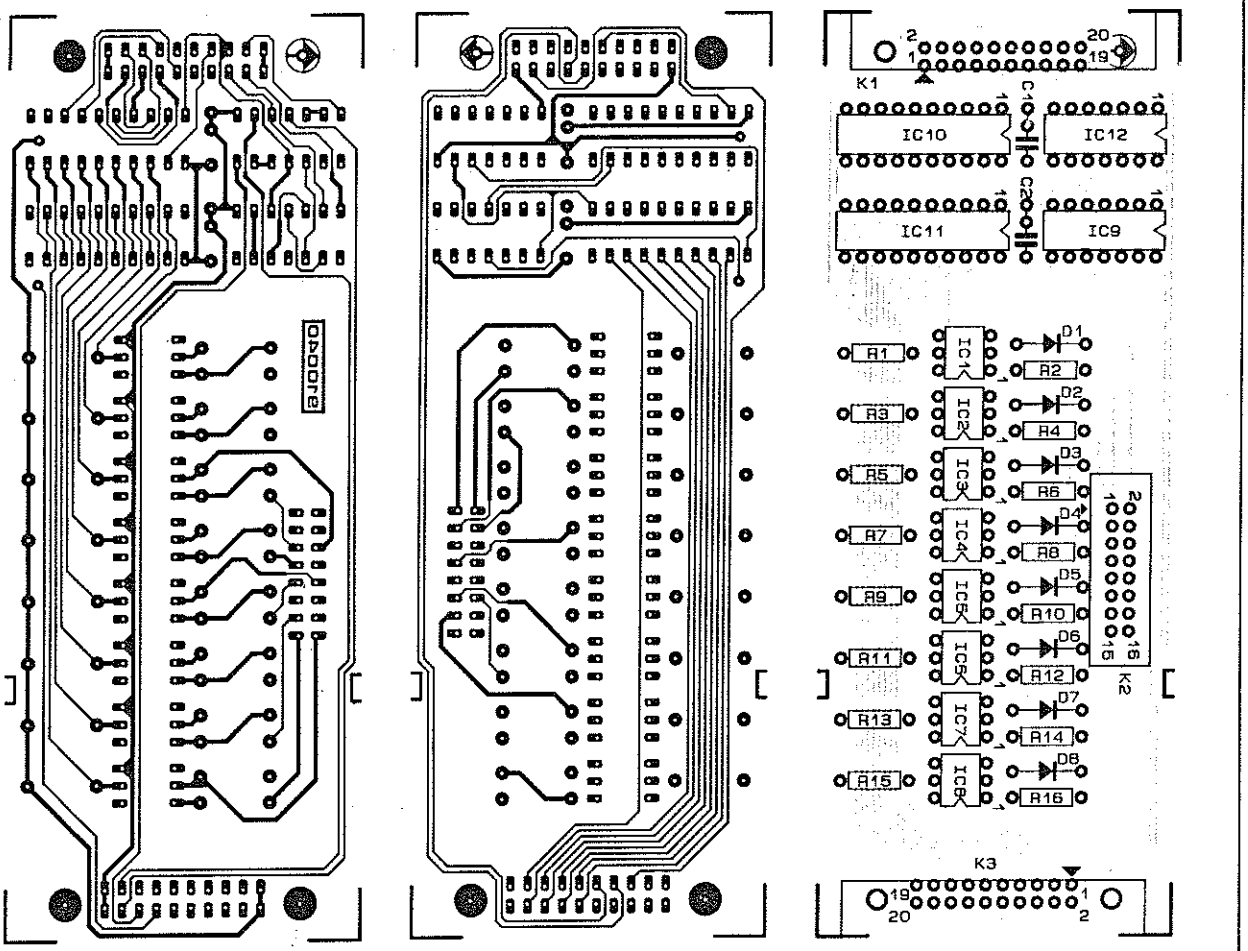


Fig. 3. Track layouts (mirror images of the component side and the solder side) and component mounting plan of the double-sided PCB for the opto interface.

cards with 'write' functions, or two cards with 'read' functions, in a position with the same card number. If you still do so, the computer will forever be unable to 'see' the card with the accented (') number. Fortunately such an 'impossible' connection will not damage the hardware, because the first card addressed in the chain keeps the $\overline{\text{ENABLE}}$ signal for the rest of the chain logic high, whereby all other extension cards are disabled.

A different kettle of fish are extension cards with read *and* write functions (we have not published any of these, but you may have ideas ...). Such cards must always be fitted in one of the first four positions, but as far as possible towards the end of the chain. If a 'read/write' card is fitted in position '1', and three relay cards in positions '2', '3' and '4', it would appear that you can not fit an opto card up to position '2'. That will not work, however, since there is first card '1', but that position is blocked by card 1. The upshot is that first four positions must always be occupied by cards that can only be read from or written to. This leaves the next positions available for cards with the double 'read/write' function.

Summarizing the above:

- the address occupied by the card is determined by its physical position in the chain;
- at every address, a distinction is made between reading and writing;
- if an address is used for writing or reading only, the corresponding accented position may be occupied by a card with the complementary function only.

■

References:

1. "Universal I/O interface for IBM PCs". *Elektor Electronics* May 1991.
2. "Relay card for universal bus". *Elektor Electronics* November 1991.

COMPONENTS LIST

Resistors:

16	1kΩ	R1-R16

Capacitors:

2	100nF	C1;C2

Semiconductors:

8	1N4148	D1-D8
8	CNY17	IC1-IC8
1	74HCT32	IC9
1	74HCT245	IC10
1	74HCT574	IC11
1	74HCT04	IC12

Miscellaneous:

2	20-way header with side latches, angled PCB connections	K1;K3
1	16-way box header	K2
1	Transparent plastic enclosure Type 222 (Heddic)	
1	Printed circuit board	910040