INTER-IC COMMUNICATIONS: THE I²C BUS

Reduction of the number of interconnections on a printed-circuit board results in lower production costs and increased reliability. Well aware of this fact, manufacturers of consumer electronics have sought ways to make inter-IC communications less complex. Philips Components have found a solution in the form of their patented I²C bus, the main features of which are described in this article.

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An increasing number of complex integrated circuits, ranging from real-time clocks to frequency synthesizers, is provided with an I²C interface. Not surprisingly, the I²C bus is found in a wide variety of electronic equipment, including telephones, car radios, television sets and video recorders.

The aim of this article is to provide an introduction into the main features and communication protocols of the I²C network. The acronym I²C stands for Inter-IC Communication, and the network was developed by Philips to reduce the number of connections between integrated circuits. This proved feasible in practice mainly because many ICs have a large number of pins that carry information that is not time-critical and, therefore, suitable for conveying via a relatively slow serial bus with fewer connections than would be required for a high-speed parallel interface. The implementation of the I²C bus on a real-time clock chip, for instance, may reduce the number of pins from 40 to as few as 8. This results in a much simpler PCB design with all the benefits of lower production cost and smaller risks of faults developing in equipment. However, a number of connections, including those for the supply voltage, for clock signals, etc., can not be replaced by a serial communication protocol. It will be clear that these connections remain necessary as before.

All ICs that use the I²C bus are in principle connected to two lines as shown in the example application in Fig. 1. A central bus interconnects two microcontrollers, a memory, a gate array and an LCD driver.

In spite of their wide diversity as regards function and application, all I²C-compatible integrated circuits have one common feature: all control commands and data are conveyed via a serial bus, according to a predefined communication protocol. The serial bus takes the form of three lines: ground, clock (SCL) and data (SDA).

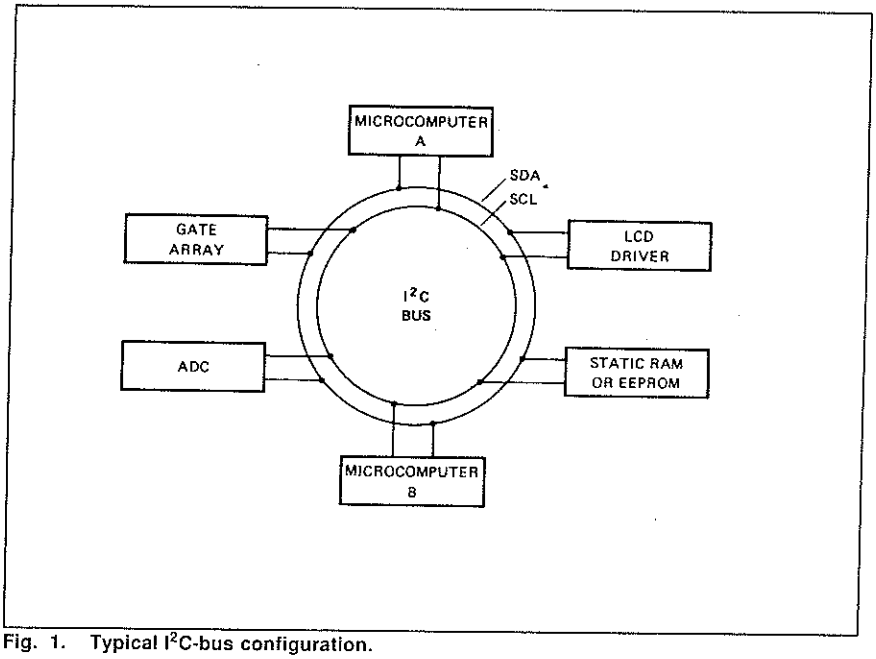

Fig. 1. Typical I²C-bus configuration.

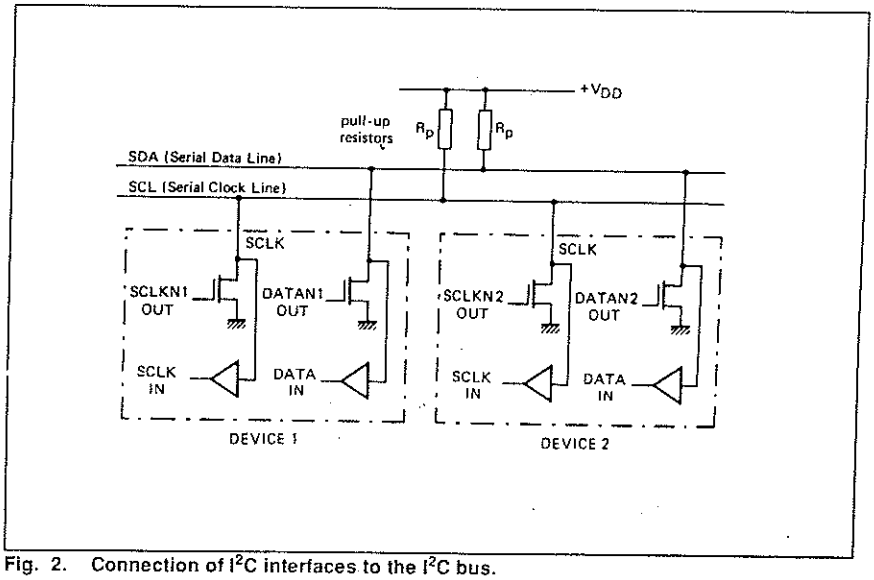

Fig. 2. Connection of I²C interfaces to the I²C bus.

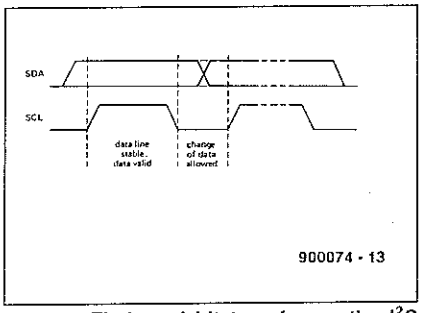

Fig. 3. Timing of bit transfer on the I²C bus.

Normally, any I²C configuration has at least one master (an IC capable of initiating the data exchange processes and generating a master clock signal) and one or more slaves (ICs that do the actual work). A master may be a microprocessor such as an 8048, an 8051 or a 68000, which are all available in special versions with a built-in I²C interface. Two I/O port lines of the microprocessor are used as SDA and SCL lines. Together with the ground line, this implements an I²C bus which allows serial communication between 'bused' devices at a data rate of up to 100 kbit per second.

Control programs for the I²C bus

The two communication lines, SDA and SCL, are connected to open-drain or open-collector outputs, and have one, common, pull-up resistor. This arrangement is called a wired-AND structure. Adding or removing one or more I²C components on the bus therefore does not affect the operation of already connected ICs, nor does it affect the software that runs on the system. In fact, the software is capable of automatic detection of the hardware configuration. This allows programs to be written for complex systems that do not provide certain features unless the relevant chips are connected to the bus. The absence of these chips is automatically detected by the master controller which interrogates certain addresses.

Existing software may be extended with subroutines written for add-on ICs without affecting the operation of the ICs already installed. This allows existing control programs to be used for a long time without the need of a completely new version every time the hardware is modified. This high level of compatibility is achieved by virtue of the fixed addresses of the ICs on the I²C bus.

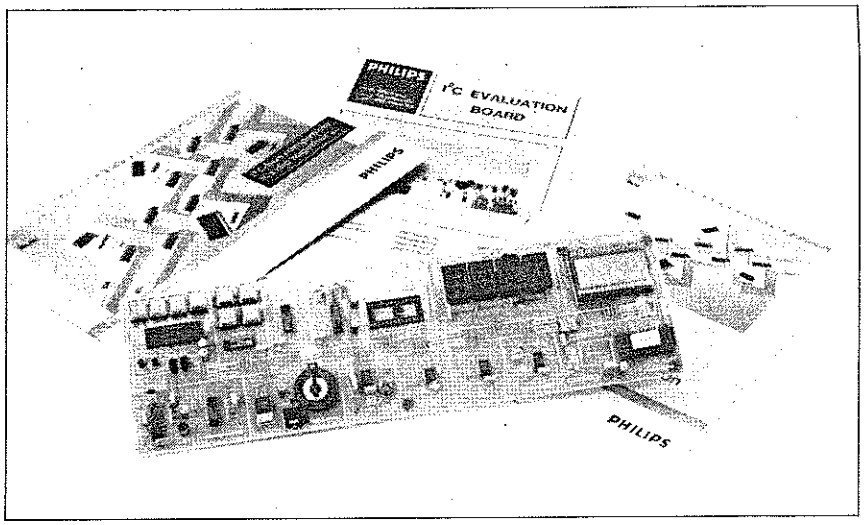

Fig. 5. Development kit for I²C applications.

Two lines

Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull-up resistor (see Fig. 2). When all output transistors of connected devices are off, the bus is free, and both lines are high. When an IC is ready to transmit a data block, it pulls SDA low to mark a start condition. From that moment, all other ICs 'know' that the bus is in use. Arbitration procedures come into effect should two or more ICs claim access to the bus simultaneously. When the start condition is recognized, the SDA line is available for carrying databits. The clock line, SCL, determines the validity of the data levels on the SDA line as shown in Fig. 3.

The start of any data exchange via the bus is marked by SDA going low while SCL is high, i.e., by a start condition (see Fig. 4). The level on the SDA line is read by all ICs on the bus during the positive part of the clock pulse. However, only the IC selected by the transmitted address code responds to the information by actually loading the data and returning an acknowledge pulse. This pulse is generated by the addressed slave device pulling the data line low for one clock period, after the eight clock periods reserved for the databits (see Fig. 4).

When none of the ICs in the system responds to the transmitted data, the master does not receive an acknowledge pulse. This means that either the addressed slave is busy performing some real-time function, the address is wrong, or there is no device that responds at the particular address. The bus is free again after the transmission of the last data bit. Both SCL and SDA revert to high, and the bus may be used to convey the next data block.

The function of the SCL line is to generate one clock pulse for every transmitted databit. Each master must generate its own SCL signal. Although the frequency of this signal is not fixed, certain minimum timing specifications must be observed. In practice, the I²C bus allows a maximum data speed of about 100 kBit/s.

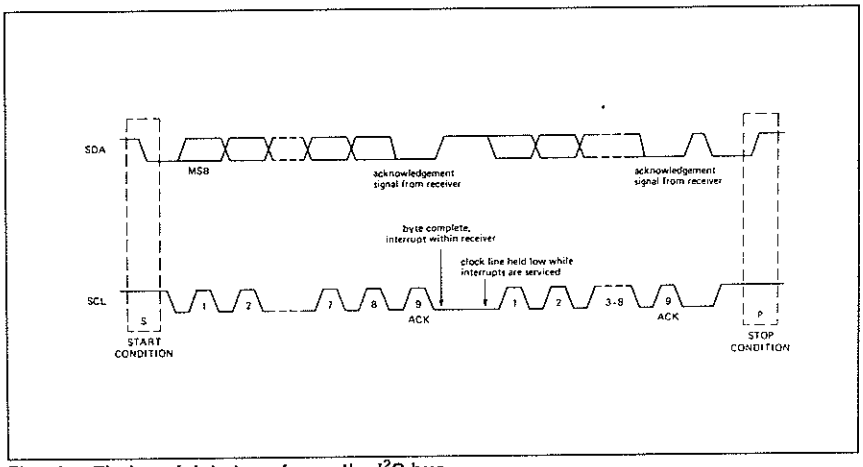

Fig. 4. Timing of data transfer on the I²C bus.

Addressing

Each IC on the I²C bus has its own, unique, 7-bit address, which is determined by the manufacturer and burned into the chip. The Type PCF8583 real-time clock chip, for example, is selected by sending the binary code 101000x. The last bit is not preset (x is 0 or 1) to allow two identical ICs to be used in parallel by tying their A0 inputs to ground or to the positive supply to set the address to 1010000 or 1010001 respectively. Similarly, certain ADCs, I/O chips and memories may be hard-wired to map them at one of up to eight addresses in a cluster.

The data blocks conveyed via the I²C

THE RANGE OF I²C-BUS COMPATIBLE ICs

General-purpose ICs

LCD drivers

PCF8566	96-segment LCD driver; 1:1 – 1:4 MUX
PCF8576	160-segment LCD driver; 1:1 – 1:4 MUX
PCF8577(A)	64-segment LCD driver; 1:1 – 1:2 MUX
PCF8578/79	Row/column LCD dot-matrix driver; 1:8 – 1:32 MUX

I/O expanders

PCF8574	8-bit remote I/O port (I²C-bus to parallel converter)
PCF8584	8-bit parallel to I²C-bus converter
SAA1064	4-digit LED driver
SAA1300	5-bit high-current driver

Data converters

PCF8591	4-channel, 8-bit MUX ADC & one DAC
TDA8442	quad 6-bit DAC
TDA8444	octal 6-bit DAC

Memory

PCA8582B	256-byte EEPROM (automotive temperature range & error correction)
PCF8570	256-byte static RAM
PCF8570C	as PCF8570 with alternative slave address
PCF8571	128-byte static RAM
PCF8582A	256-byte EEPROM

Clocks/calendars

PCF8573	clock/calendar
PCF8583	256-byte RAM/clock/calendar

Application-oriented ICs

Video/radio/audio

PCF8200	voice synthesizer (male/female speech)
SAA1136	PCM-audio Ident word Interface (IDI) for compact disc
SAA1300	tuner switching unit
SAA3028	transcoder (RC-5) for IR remote control
SAA4700	data line processor for VPS
SAA5243*	enhanced computer-controlled teletext (ECCT) processor
SAA9050/51	digital PAL/NTSC colour decoder
SAA9055	digital SECAM decoder
SAA9062/63/64	digital deflection controller
SAA9068	picture-in-picture (PIP) controller
SAB3035/36/37	digital tuning circuits for computer-controlled TV
SAF1135	dataline-16 decoder for VCR
TDA8405/15	stereo/dual sound processor
TDA8421	audio processor with a loudspeaker channel and a headphone channel
TDA8425	audio processor with a loudspeaker channel only
TDA8433	deflection processor and sync controller
TDA8440	video/audio switch
TDA8461	PAL/NTSC colour decoder and RGB processor
TEA6100	FM/IF and digital tuning IC for computer-controlled radio
TEA6300	sound fader control and preamplifier/source selector for car radio
TEA6310T	sound fader control with tone and volume control for car radio
TSA5510	PLL frequency synthesizer for TV and VCR
TSA6057	PLL frequency synthesizer for radio

Telecomms

PCD3311/12	tone generator (DTMF/modem/music)
PCD3341	advanced 10/110-number repertory pulse/DTMF dialler with LCD control
PCD3343	microcontroller with 224-byte RAM/3K ROM
PCD3346	microcontroller with 128-byte RAM/4K ROM/256-byte EEPROM
PCD3348	microcontroller with 256-byte RAM/8K ROM
UMA1000T	data processor (DPROC) for mobile telephones
UMA1010T	frequency synthesizer (0.45 – 1.1 GHz) for mobile telephones
UMA1012T	frequency synthesizer (50 – 600 MHz) for mobile telephones

Table 1. Overview of I²C-compatible integrated circuits manufactured by Philips Components. Not shown here is a wide range of microcontrollers and memories.

bus invariably consist of 8 bits. The bit that follows the address indicates the start of a read or a write operation with the selected IC. Bit 8 is low for a write operation, and high for a read operation.

Applications

There is much more to the concept of the I²C bus than can be described in this article. The full specification of the system may be found in Ref. 1.

The I²C bus is relatively simple to implement on almost any microcomputer system that has at least one user port. If necessary, external buffers may have to be added to make such a port bidirectional. Interestingly, Philips Components recently introduced a special chip for this purpose: the PCF8584. Some microcomputers, including the Acorn Archimedes, even have an I²C interface as a standard feature. Developers of small stand-alone microprocessor systems may find the I²C version of the 8048, the PCF84C00T, a good starting point for the design of a dedicated control system.

Finally, an interesting example of the use of a 8051 microcontroller in combination with the SAA5243 I²C-bus Teletext decoder may be found in Ref. 2. ■

Fig. 6. Databooks on I²C devices, published by Philips Components.

Reference:

1. *The I²C-bus Specification.* Philips Components publication.
2. *Computer-controlled teletext decoder.* Elektor Electronics October 1989