

# A SIMPLE WATCHDOG CIRCUIT

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**S**INGLE-CHIP microcontrollers have been designed and optimized for specific applications such as industrial control and automotive applications. The Intel MCS-51 family of microcontrollers is a popular and typical example.

The presence of various types of electrical noise and interference in the above mentioned applications is by no means taken for granted, but generally accepted as hard to avoid. By virtue of some special features, such as powerful Boolean processing capabilities, single-chip microcontrollers are mostly used in industrial control applications which are known as electrically noisy environments.

In spite of a well-designed power supply, a shielded enclosure, and adequate decoupling provisions, noise may still enter a microcontroller system, upsetting the normal operation, or even causing a system crash. These situations are usually marked by the microprocessor going into its static state, or performing unpredictable operations. In such a case, normal operation can be restored only by a hardware reset (PC users know this as BRST — Big Red Switch Time).

A problem occurs when the microprocessor system operates unattended, which is usually the case in industrial applications. A total lockup of the system can then disrupt a production line, or cause expensive 'down time'. In such applications, hardware resetting must be performed automatically on detection of a software malfunction. The circuit described here (Fig. 1) provides a simple method to accomplish this.

## Circuit description

The watchdog circuit consists of a power-up reset, a gated astable multivibrator, and a failure detector circuit. In fact, the total circuit simulates a retriggerable monostable

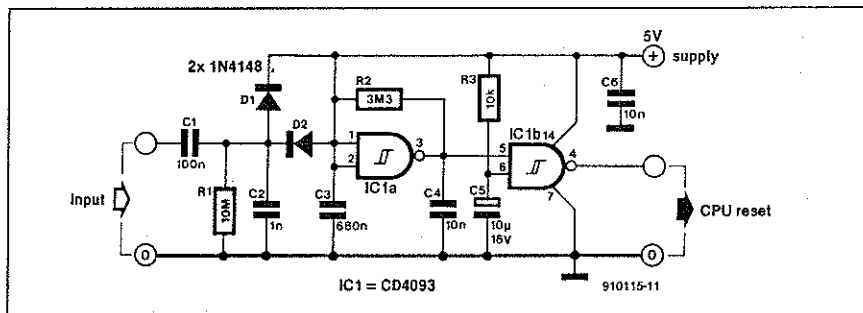


Fig. 1. Circuit diagram of the watchdog. The input is connected to a CPU port line.

multivibrator, which detects a software upset whenever it is not triggered at a proper rate.

In the MCS-52 family of microcontrollers, PX.X can be any pin (bit) of the ports 1, 2 or 3. Ports 2 and 3 may not be used when performing their secondary functions. Components R3 and C5 form a power-up reset circuit that applies a reset pulse to the CPU via gate IC1b, whenever power is applied.

During normal operation, and in the main loop of the program, a periodic pulse must appear on port line PX.X. The frequency of this signal must be at least 10 Hz. The software determines which port line is used to keep the watchdog triggered. In 8051 assembler code, this is simple to implement by the instruction CPL PX.X, where X.X is the port line identification, e.g. 1.0 (bit 0 of port 1).

The software failure detector consists of C1, R1, D1 and D2. The pulse train applied to the PX.X input of the circuit continuously discharges C3 via D2 and C1. As a result, the gated bistable around gate IC1a is disabled, and its output goes high. Hence, during normal program execution, the two inputs of IC1b are high, so that the CPU reset line is held low.

As soon as a software upset occurs, the

CPU very likely leaves the main loop of the program. This means that the pulses on PX.X fail, so that the port line takes on a static level. This enables the astable circuit which consists of IC1a, R2 and C3. After C3 has been fully charged by R2, the output of IC1a goes low. Consequently, a logic high reset pulse appears at the output of IC1b.

Because IC1a functions as an astable multivibrator, C3 is discharged again after about one second, so that the output of IC1a goes high. This causes the CPU reset line to revert to logic low, and the control program is executed starting at the reset address. The CPU has enough time (about one second) to restart the pulse train on PX.X, and resume its normal operation.

The reaction time of the watchdog may be shortened by using a smaller capacitor in position C3. Capacitors C2 and C4 reduce the effect of noise on the operation of the circuit. If a reset key is required, you can connect a pushbutton in parallel with capacitor C5.

This circuit may also be used with any of the devices in the Intel MCS-48 family of single-chip microcontrollers. This, however, requires an inverter gate to be inserted between the output of IC1b and the CPU reset line, because these controllers have active-low reset inputs.

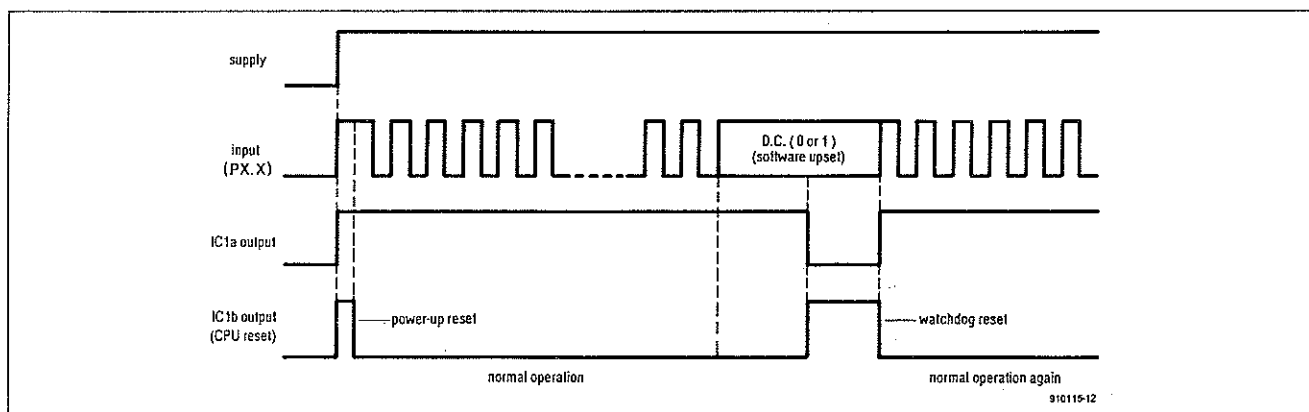


Fig. 2. Ideal waveforms illustrating the operation of the watchdog circuit.