compression characteristic is shown in Fig. 2. The signal range is reduced by about one half at the output, which is doubled in the expander. This means that the range after compression and expansion is the same again, but that is not necessarily the case with the input and output level. The compander may be arranged to provide a constant attenuation or amplification. With the circuit values as shown in the diagram, the input and output levels are the same. The prototype had an overall gain of 0.5 dB when the expander input was connected direct to the compressor output.

To allow acceptance of high input levels, R13, R14 and the compressor input resistance form a 10:1 attanuator. At the expander input, R5 and the expander input impedance of about 3 kΩ form a potential divider. If the compander is to be used with smaller signals, the attenuation may be reduced as appropriate. If the input level lies below 100 mV, R5, R13 and R14 may be omitted.

The compander covers the frequency range of 20 Hz to 20 kHz; the overall distortion is less than 1%; and the signal-to-noise ratio is about 80 dB. ■

(T. Giffard)

LIQUID CRYSTAL DISPLAY FOR 8052 MICROCONTROLLER

040

The display is intended to be added to the address and data bus of the Type 8052 microcontroller. Liquid crystal displays come in a number of varieties: in the prototype a two-row, 16 characters per row type was used, which, moreover, contains two registers.

The signals on the RD and WR lines of the controller are too short to enable data to be written into, or read from, the display registers. The way this problem is resolved consists of using the lowest value address bit, A0, to verify whether a write or a read action is required. The address signals last long enough for completing a data exchange with the display. The next highest address line, A1, is used to differentiate between the data register and the instruction register of the diaplay.

Then:

Basic address: write data into instruction register;

Basic address +1: read contents of instruction register;

Basic address +2: write data into data register;

Basic address +3: read contents of data register.

The basic address, which must be a multiple of 4, is determined by the chip select (CS) signal of the controller.

The enable signal for the display is derived from the CS signal, the RD and WR signals, and address signal A0.

These functions are carried out by a Type 74LS151 IC. This device prevents a spurious address to be read or written and so avoids a conflict between the buses. Only when the display is addressed by CS when either RD or WR are logic low will the address line A0 give an enable signal. The 74LS151 may be replaced by the corresponding HC or HCT type.

If more protection for the controller is required, the data bus may be expanded by a bus driver, for which a bidirectional buffer, such as Type 74LS245, is required. The direction of transfer is determined by the lowest value address line, A0, and the linking of the enable signal with the W signal of IC1. ■

(J. Romanus)