50 MHz 8-BIT DAC

The digital-to-analogue converter described here is fast, based on discrete components, and comparable — in terms of performance — to pretty expensive integrated circuits.

by R. Shankar

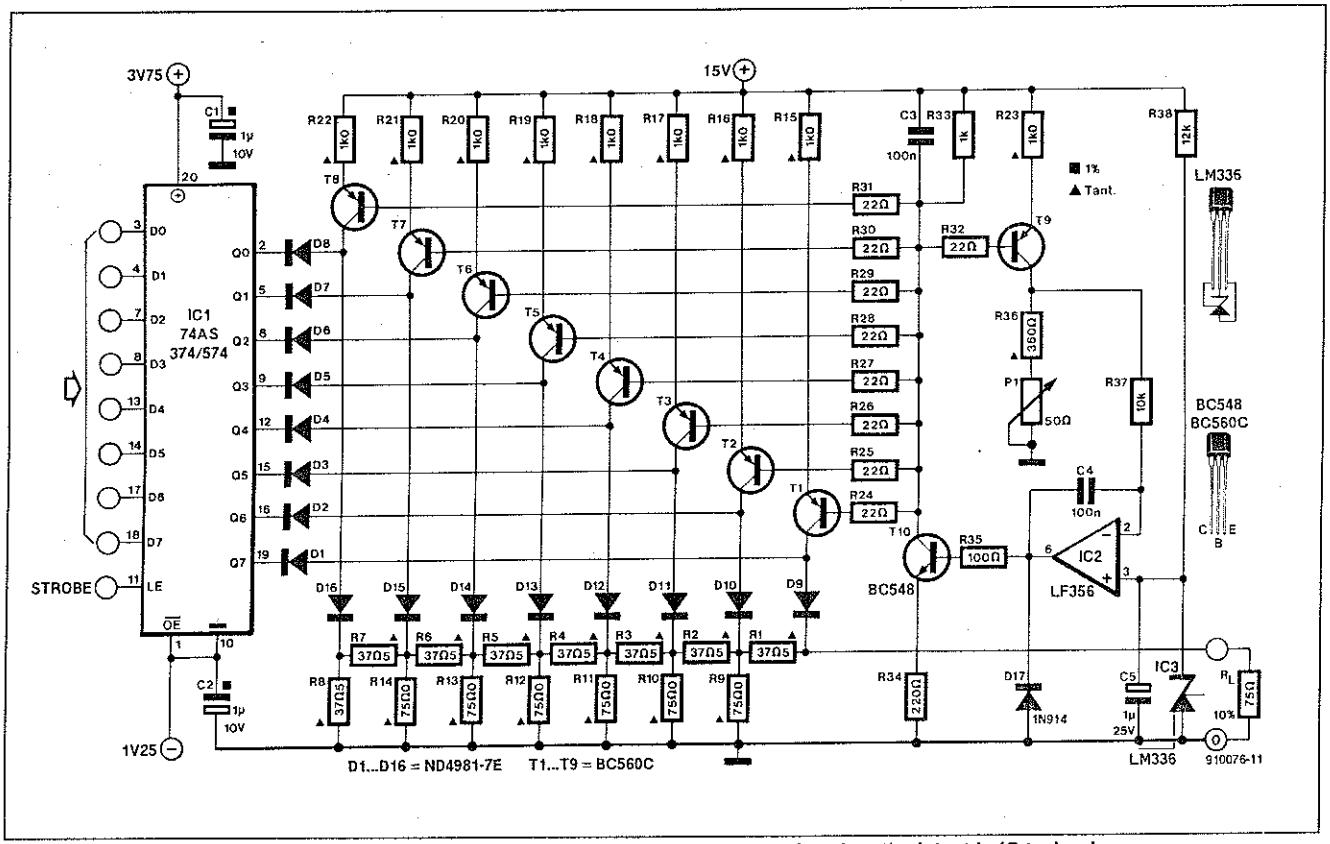


Fig. 1. This fast digital-to-analogue converter is based on discrete components rather than the latest in IC technology.

THE converter can directly drive a 75-Ω load at a full scale voltage of 0.510 V, and a settling time of less than 10 ns to 1 LSB. The temperature coefficient of the output voltage is 0.005%/K, which is significantly better than that of many integrated DACs.

The circuit is based on the conventional *R-2R* ladder network, with current switching accomplished by Schottky diodes and a high-speed Advanced Schottky (ALS) TTL latch. Resistors R1 to R14 form the ladder network, the output impedance of which is 75 Ω. This enables the DAC to drive a load via a 75-Ω coax cable.

Transistors T1 to T8 form the current sources that supply 6.67 mA each to the ladder network via D9 to D16. When any output of IC1 goes low, the resulting current is diverted to IC1 via D1 to D8. This arrangement requires the outputs of IC1 to go negative with respect to ground. Therefore, IC1 is operated with a dual supply of –1.25 V and +3.75 V. To make the inputs TTL compatible, a level translator like the one shown in Fig. 2 may be used at each input. The input loading ('fan-in') of the translator is equal to that of 3 standard TTL inputs. The circuitry around T9, T10, IC2 and IC3 is necessary to obtain a low temperature coefficient.

A suggested power supply circuit is shown in Fig. 3. The current consumption of the DAC is of the order of 170 mA.

Construction hints

Although no PCB design is available for this project, the construction is fairly simple even on a prototyping board. D1 to D16 can be any Schottky diode that meets the following specifications: $I_{Dmax} \geq 10$ mA; $V_{BR} \geq 5$ V; $V_f \leq 0.5$ V at 10 mA.

The connections of the ladder resistors, the Schottky diodes, IC1 and C2 should be kept as short as possible. A large ground

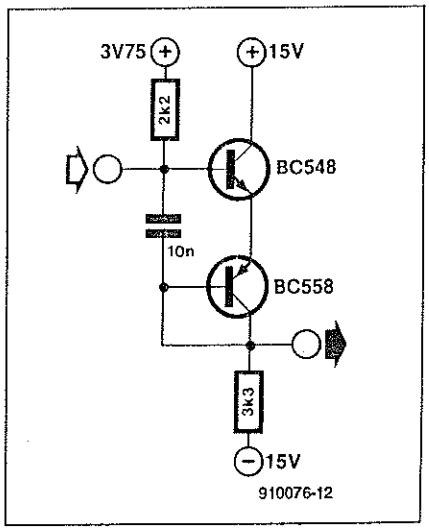


Fig. 2. TTL-compatible input level translator.

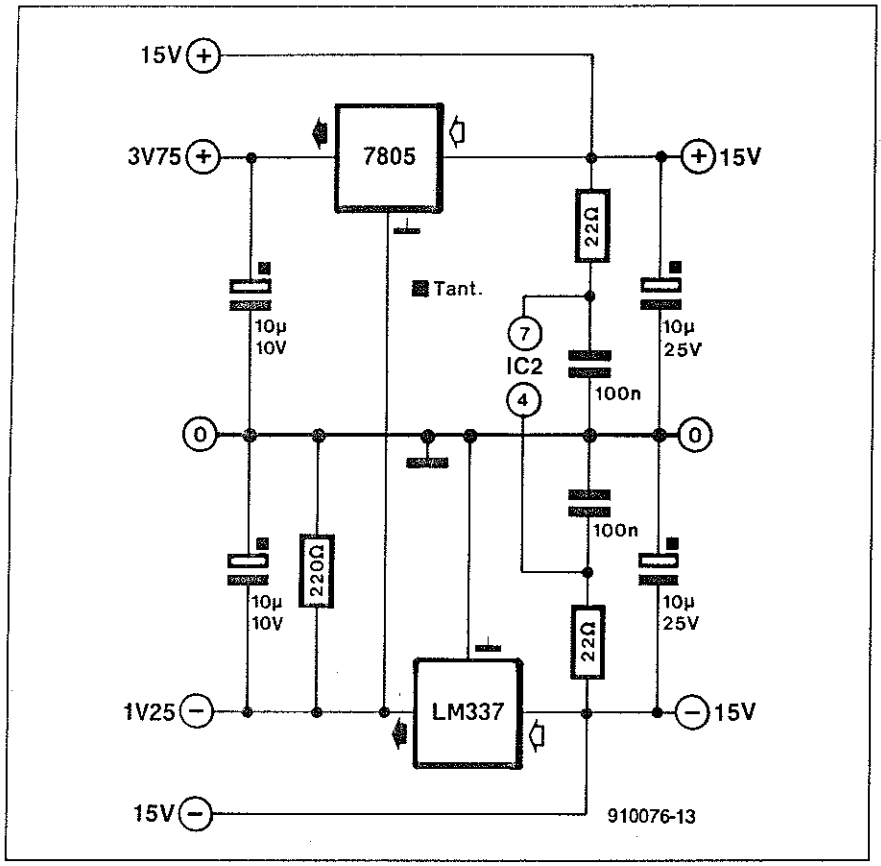
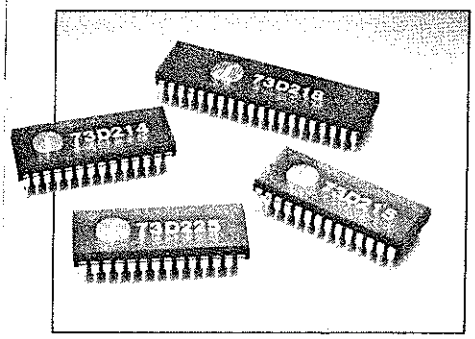


Fig. 3. Regulated power supply for the DAC.

plane should be provided, and the earthed ends of R8-R14, R1 and C2, should meet at one point.

Without component matching, the linearity is of the order of 2 LSB. However, by carefully matching the resistors with the aid of a digital multimeter, a linearity of better than 0.5 LSB can be achieved (tip: use the closely matched resistors towards the MSB). Similarly, the transistors can be matched by measuring the resistance of the base-emitter junction, and noting the values. This measurement should be carried out with the collector and the base connected via the test probe. Additionally, T1 to T9 may be mounted on a common heat-sink for close thermal tracking. ■

Popular modem IC set upgraded to include FAX



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TVRO analysis and dish aiming software

Greg Grissoms' *TVRO System Analysis and Antenna Aiming Computer Programs for Satellite Technicians* is a software package aimed at satellite TV enthusiasts, professionals as well as TVRO dealers. It can also be a useful adjunct in demonstrating how changing parameters such as dish size or LNB noise figure affect picture quality.

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