SCIENCE & TECHNOLOGY

Augmented *A*-matrices:

a new circuit technique suitable for use with home computers

by Michael Soper, MA

Many articles have been written on the use of two-by-two matrices for the representation of two-port or four-terminal networks. Computer design now makes such techniques seem laborious when CAD facilities are available. But many designers still do not have access to such advanced facilities and need powerful techniques to help them analyse their proposed circuits. The advantage of the techniques outlined in this paper is that, unlike standard matrix techniques, they may represent forward-biased diodes as well as linear active or passive circuits.

To describe the system, we start off with the standard circuit where a shunt impedance Z has these equations:

$$V_1 = V_2$$

and

$$I_1 = V_2/Z - I_2$$

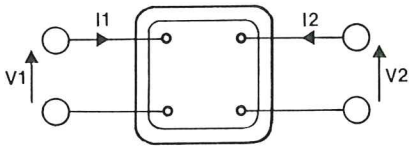
and is represented by the matrix

$$\begin{bmatrix} 1 & 0 \\ 1/Z & 1 \end{bmatrix}$$

The whole standard system is summarized as follows:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = [A] \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}$$

represents this circuit



910058 - 11

where

$$A = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix}$$

and the circuit equations are:

$$V_1 = a_{11} V_2 - a_{12} I_2$$

$$I_1 = a_{21} V_2 - a_{22} I_2$$

The system in use here is a three-by-three matrix system which represents these equations:

$$V_1 = a_{11}V_2 - a_{12}I_2 - u.1$$

$$V_2 = a_{12}V_2 - a_{22}I_2 - y.1$$

$$1 = 1$$

The third equation is purely formal and thus the three-by-three matrix has this form:

$$\begin{bmatrix} a_{11} & a_{12} & u \\ a_{12} & a_{22} & y \\ 0 & 0 & 1 \end{bmatrix}$$

Another notation may be used for this:

$$\begin{bmatrix} a & b & u \\ c & d & y \\ 0 & 0 & 1 \end{bmatrix}$$

The vectors to use are:

$$\begin{bmatrix} V \\ I \\ 1 \end{bmatrix}$$

This is the standard voltage/current vector used in transmission matrices augmented by the extra column:

$$\begin{bmatrix} u \\ y \\ 1 \end{bmatrix}$$

All this will be explained more fully in the following.

A drawback of *A*-matrix technique is that although linear passive circuits can be represented adequately for design purposes by two-by-two matrices (called *A*-matrices), these are not adequate for the d.c. design of active circuits. This is because of the necessity of bias components which can not be calculated by what is essentially an incremental method. For example, there is unfortunately no matrix for a forward biased silicon diode.

This restriction has its origin in the mathematical fact that two-by-two matrices can not be used to move the origin to which the

$$\begin{bmatrix} V \\ I \end{bmatrix}$$

vectors of the model are referred. This restriction may be removed by an artifice: replace

$$\begin{bmatrix} V \\ I \end{bmatrix} \text{ by } \begin{bmatrix} V \\ I \\ 1 \end{bmatrix}$$

and use three-by-three matrices. These may be termed 'augmented' A-matrices and they have the form:

$$\begin{bmatrix} a & b & u \\ c & d & z \\ 0 & 0 & 1 \end{bmatrix} \qquad [1]$$

where u, z are complex numbers as are, of course, a, b, c, d.

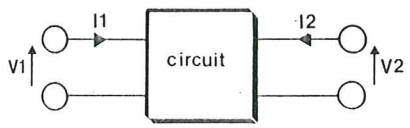
Standard *A*-matrix technique

We will summarize the standard *A*-matrix technique and then show how the augmented matrices are an improvement.

A-matrix technique has its origin in the equations:

$$V_1 = aV_2 - bV_2 \qquad [2a]$$

$$I_1 = cV_2 - dV_2 \qquad [2b]$$



910058-12

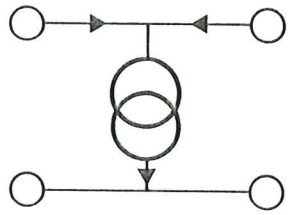
where V_1, I_1 are the input voltage and current, and V_2, I_2 are the output voltage and current. Equations [2a] and [2b] may be summarized neatly in matrix form:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = [A] \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \qquad [3]$$

The simple series impedance, Z, and the parallel admittance, *Y*, have therefore the corresponding *A*-matrices:

$$\begin{bmatrix} 1 & Z \\ 0 & 1 \end{bmatrix} \quad \begin{bmatrix} 1 & 0 \\ Y & 1 \end{bmatrix} \qquad [4]$$

A formulation like this is particularly suitable for use in computer programs, but it has a serious limitation: *V* and *I* are incremental, not absolute, as may be seen from the fact that a shunted current-source can not be represented by an *A*-matrix.



$$\begin{bmatrix} ? \\ ? \end{bmatrix}$$

910058-13

New system

The liberation of the standard technique from this restriction is relatively easy, since the restriction has its root in the fact that two-by-two complex matrices can not be used to represent translations in the (V, I) plane. The solution is to replace each vector

$$\begin{bmatrix} V \\ I \end{bmatrix} \quad \text{by} \quad \begin{bmatrix} V \\ I \\ 1 \end{bmatrix}$$

and each matrix *A* by:

$$\begin{bmatrix} A & \begin{matrix} u \\ Z \end{matrix} \\ 0\ 0\ 1 & \end{bmatrix} \qquad [5]$$

To give an example: suppose the circuit is

$$I_1 = cV_2 - dV_2 \qquad [2b]$$

in which the diode is forward biased and has zero forward impedance. The matrix for a silicon diode then summarizes the situation:

$$\begin{bmatrix} 1 & 0 & 0.7 \\ 0 & +1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

and

$$\begin{aligned} V_1 &= V_2 + 0.7 \\ I_1 &= -I_2 \\ 1 &= 1 \end{aligned} \qquad [6]$$

Current source

Let us now consider the matrix of a current source

$$\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & -i \\ 0 & 0 & 1 \end{bmatrix} \qquad [7]$$

which provides these equations:

$$\begin{aligned} V_1 &= V_2 \\ I_1 &= -I_2 - i. \end{aligned}$$

The source has infinite impedance and supplies a current *i*. These matrices may be multiplied just as the unaugmented matrices: the result represents two circuits in cascade. The advantage of this system is that it is absolute and can represent absolute levels of voltage and current.

To model a transistor, we must include the knee voltage of the emitter-base junction and an emitter-collector working voltage. A small-signal silicon n-p-n transistor with a 0.7 V e-b voltage in a common-emitter configuration might have a matrix

$$\begin{bmatrix} -7\times 10\text{E}-4 & -20 & 0.7 \\ -10\text{E}-6 & -0.24 & 10\text{E}-6 \\ 0 & 0 & 1 \end{bmatrix}$$

When it is known what d.c. voltage offsets are required at input and output, the matrix may be computed as follows:

$$M = \begin{bmatrix} 1 & 0 & V_{\text{knee}} \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} A & \begin{matrix} 0 \\ 0 \end{matrix} \\ 0\ 0\ 1 & \end{bmatrix} \begin{bmatrix} 1 & 0 & -V_{\text{w}} \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

If the matrix is to represent a transistor, and *A* is the usual *A*-matrix for, say, a common-emitter configuration, *A* may be found from the *h* parameters, where *h* is the determinant of the hybrid matrix by choosing

$$\begin{aligned} a &= -h/h_{21} \\ b &= -h_{11}/h_{21} \\ c &= -h_{22}/h_{21} \\ d &= -1/h_{21}. \end{aligned}$$

Empirical tests may be the best way to obtain optimum parameters for the augmented *A*-matrix.

A related question is: 'Given the augmented *A*-matrix of a transistor, how can the surrounding circuit values be designed?'

In a common-emitter configuration, the emitter resistor, the collector resistor, and the two base bias resistors are the minimum requirement.

This is best shown by an example as follows.

Design procedure

In the design of a small-signal, single-stage n-p-n bipolar silicon transistor amplifier in a common-emitter configuration, let *A* be the augmented matrix of the transistor. For convenience, we write the column vectors in rows.

1. Solve $A(Z, 0, 1)^T = (V_k, 0, 1)^T$

for V_k, where *Z* is adjusted for zero input current.

Then, let the supply voltage be *V* and the transistor d.c. current, *I*.

$$A \begin{bmatrix} 1 & R_L & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} [V, -I, 1]^T = [0.7, I/\alpha h_{22}, 1]^T$$

2. Solvefor R_L.

3. Let *j* be the current in the potential divider and dv half the peak-to-peak signal value; then:

$$\begin{bmatrix} 1 + R_2/R_1 & R_2 & 0 \\ 1/R_1 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

$$[0.7 + \text{d}v, -I/\alpha h_{22}, 1] = [V, j, 1]$$

Solve for R_2 and R_1.

System use

The use of this system has been outlined in the foregoing; it allows, with care, circuits containing forward- or reverse-biased diodes and transistors, as well as passive components, to be easily designed. ■

References.

"Matrix Algebra - 2" by G.H. Olsen, *Wireless World*, April 1965.

"Useful matrix theorem with applications to electronic circuit theory" by M.C. Soper, *Electronics Letters* (IEE), 18 July 1985, Vol. 21 No. 15.

"Electromagnetism and Time" by M.C. Soper, *Awareness*, Vol. 12 No. 2, 1983-84.

Introductory circuit theory by Guillemin, Wiley 1953.

"Metalogic" by M.C. Soper, *Awareness*, Vol. 16, No. 3, 1989.